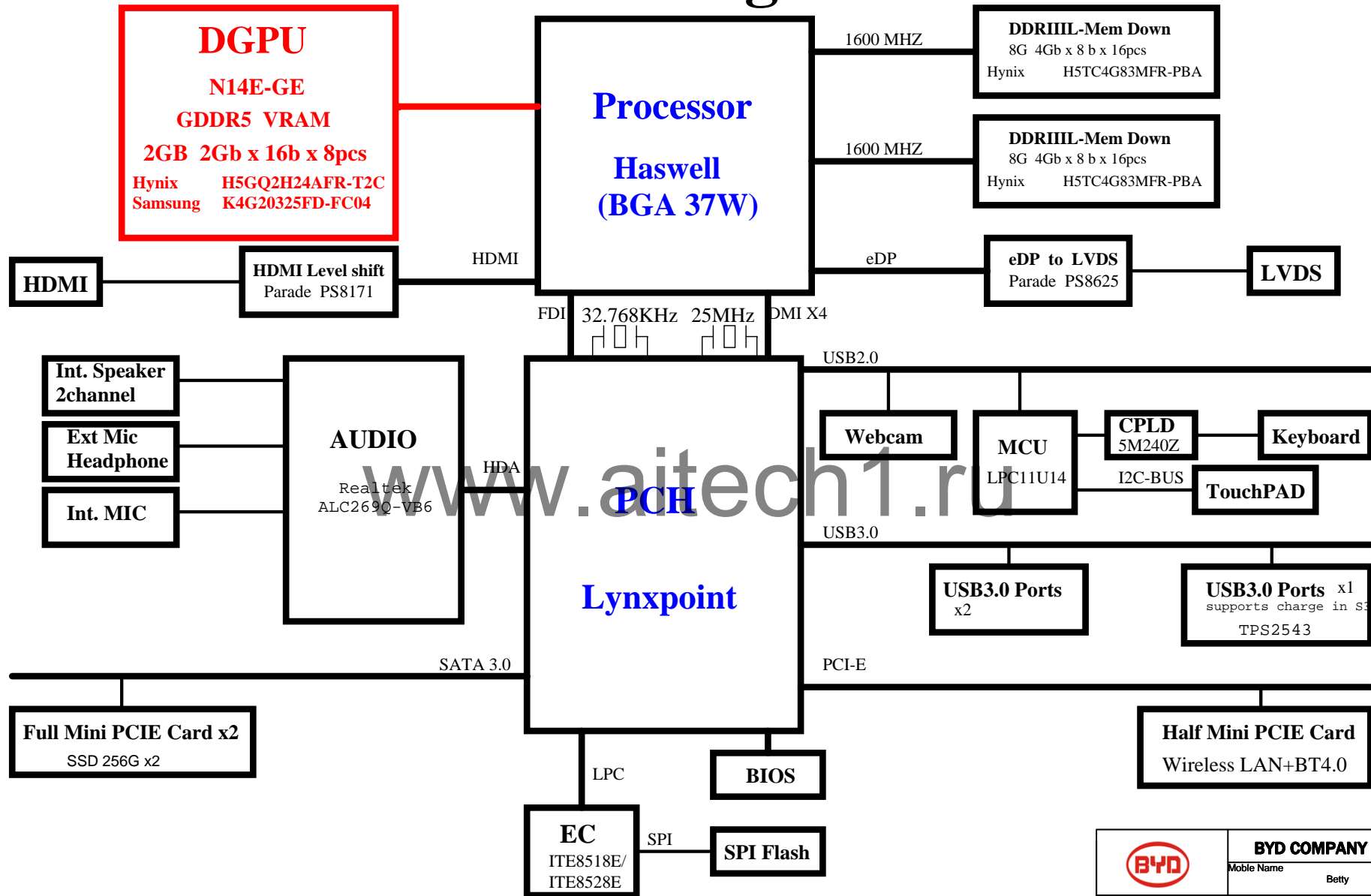
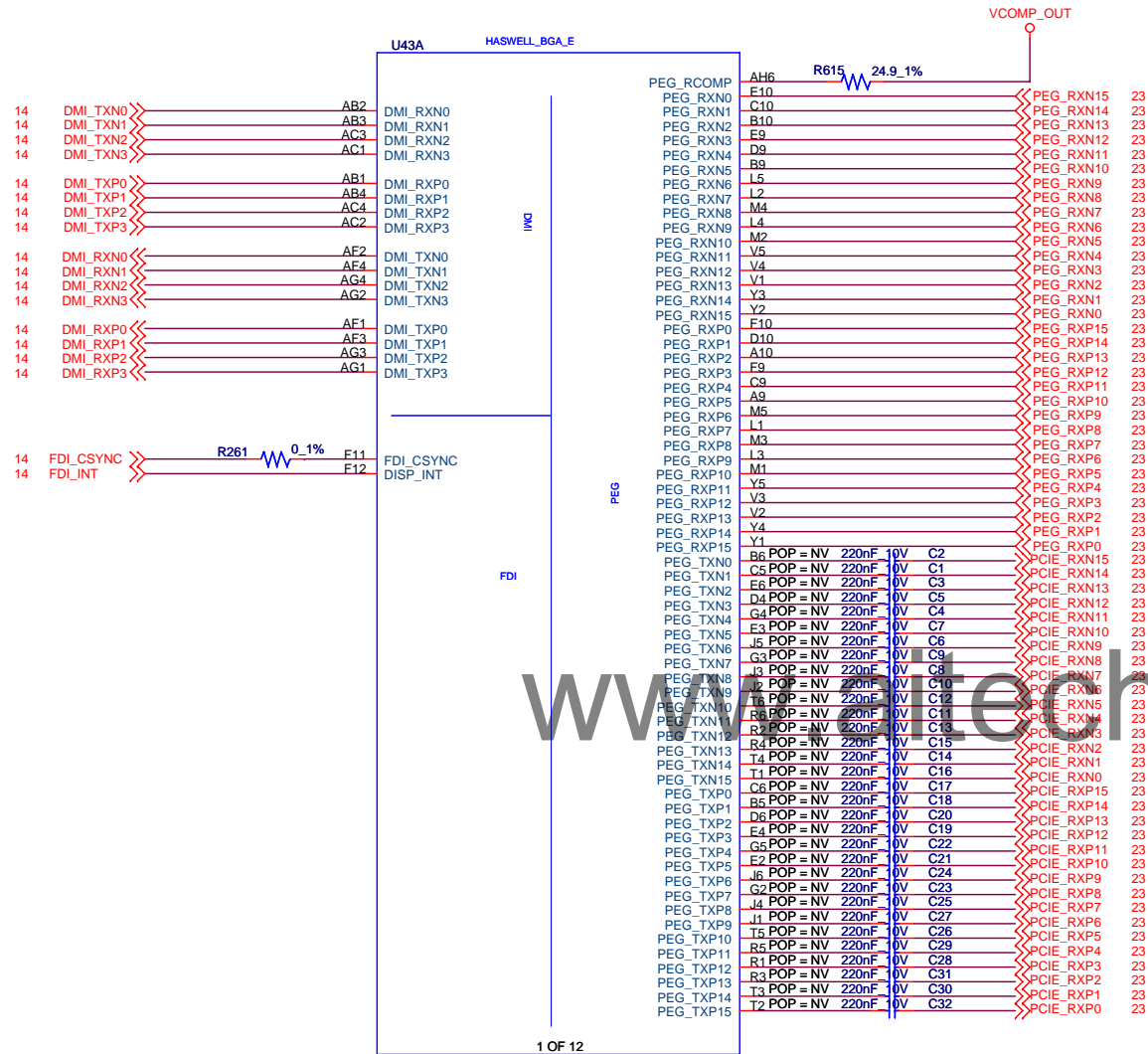
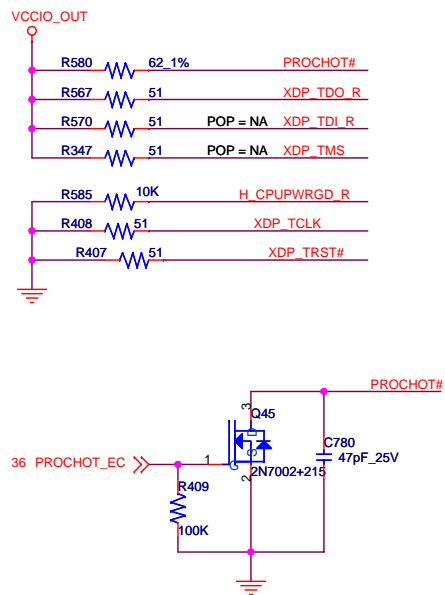
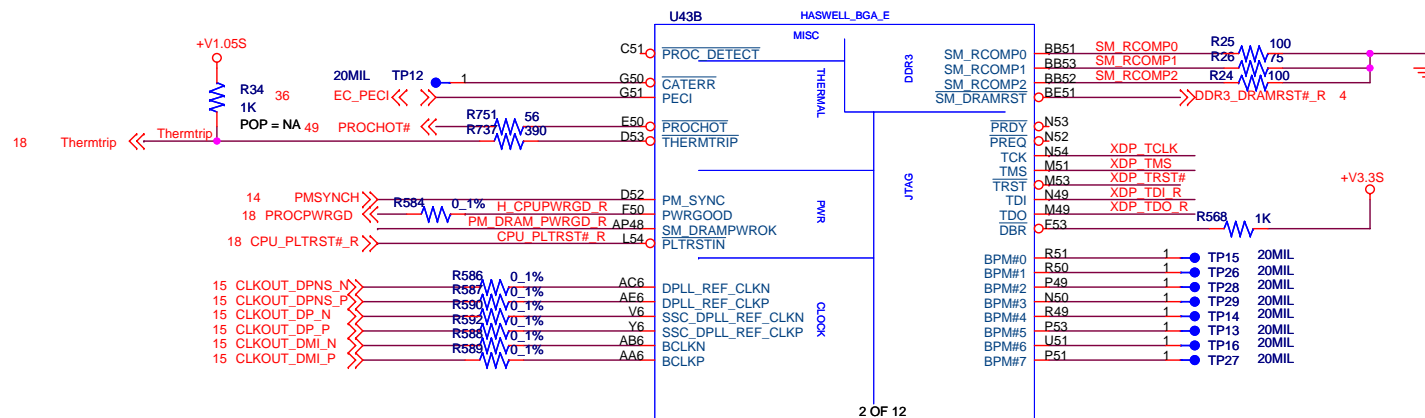


Block Diagram



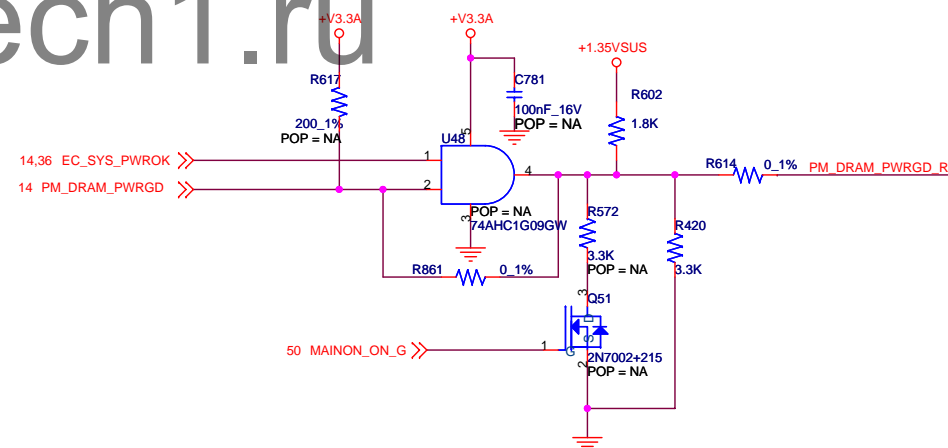
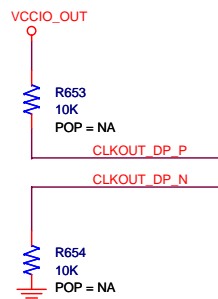


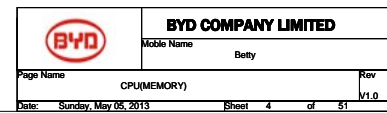
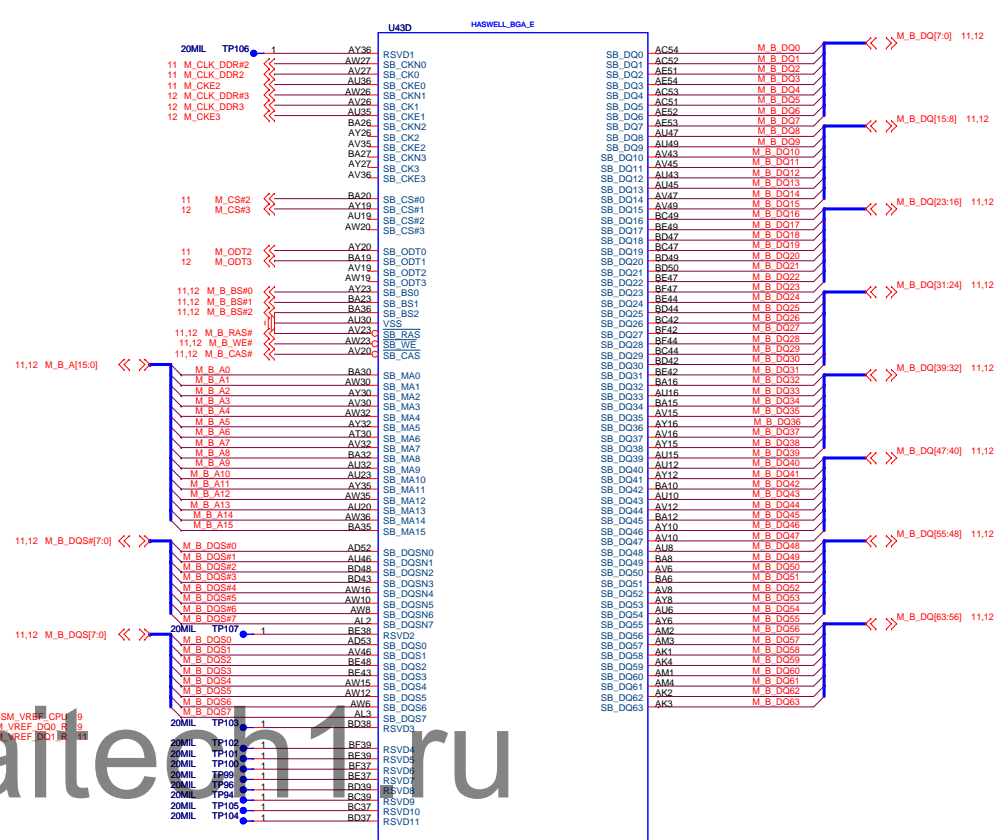
www.fitech1.ru

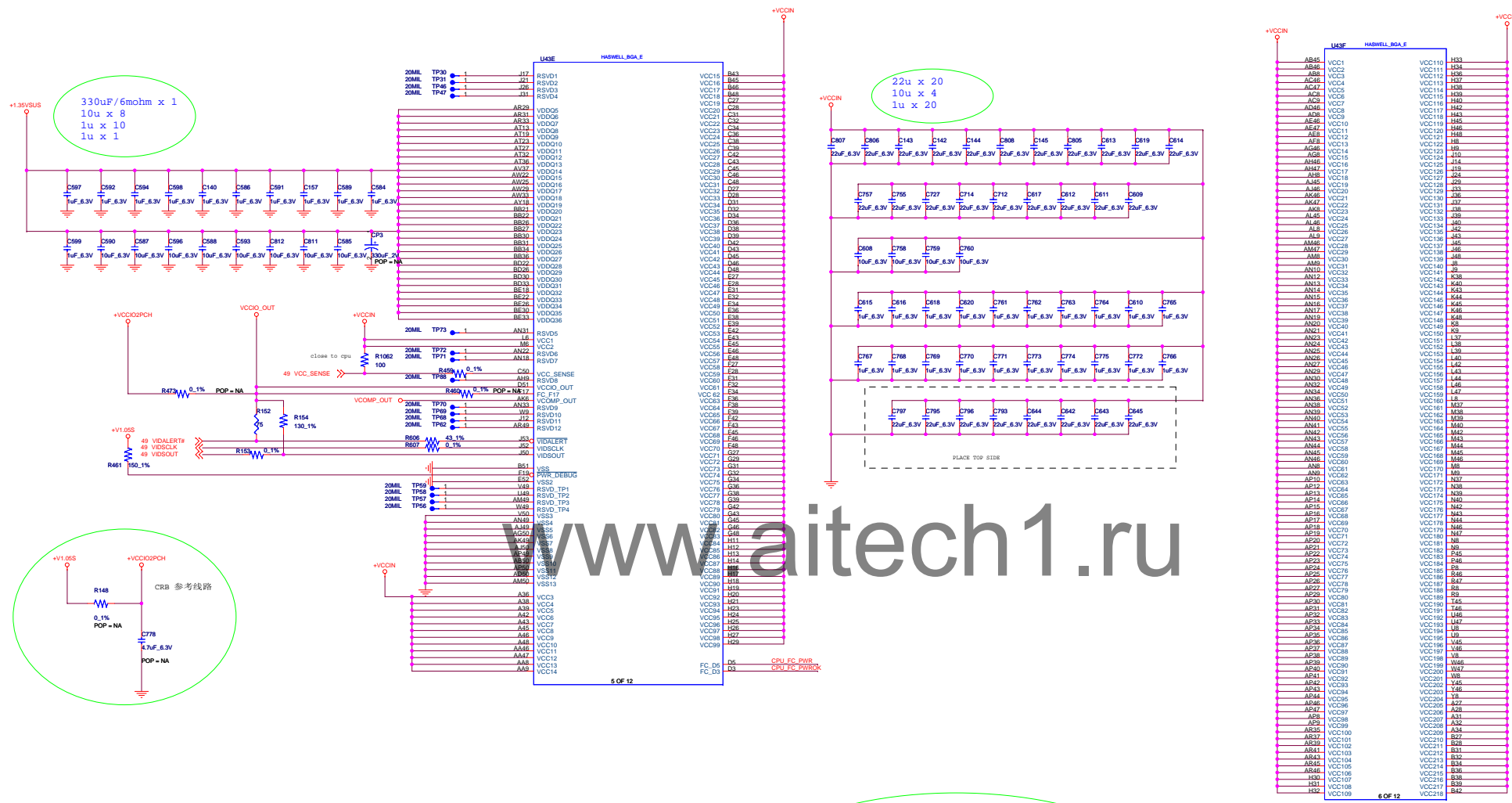


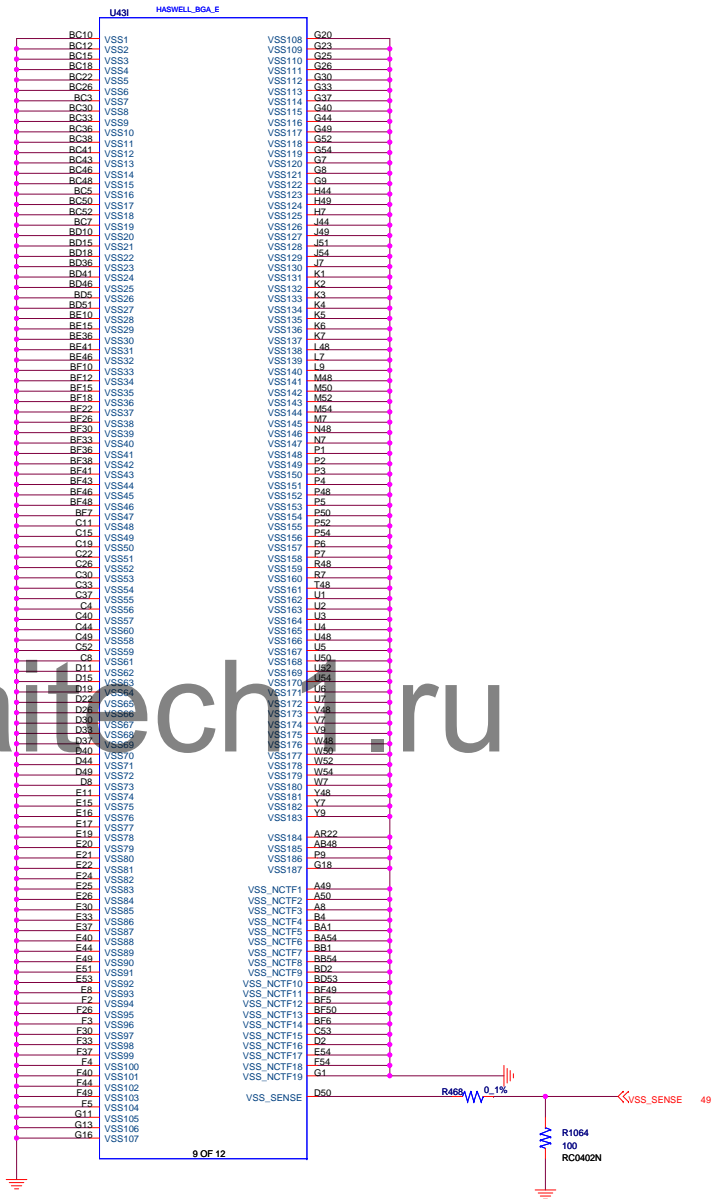
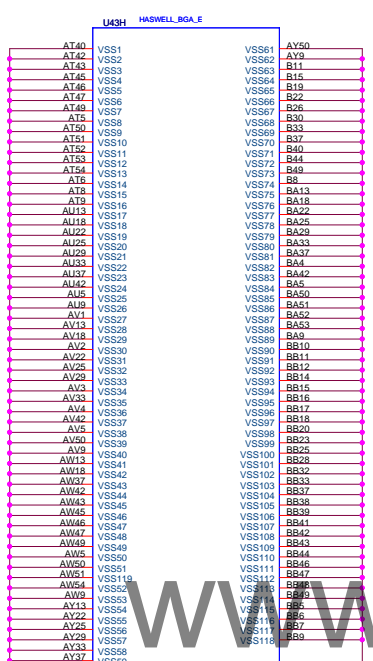
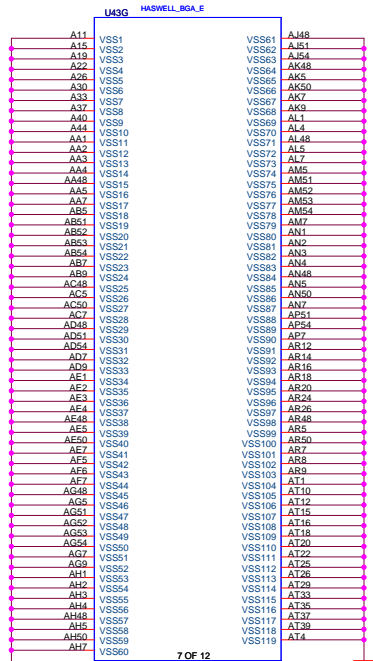
www.aitech1.ru

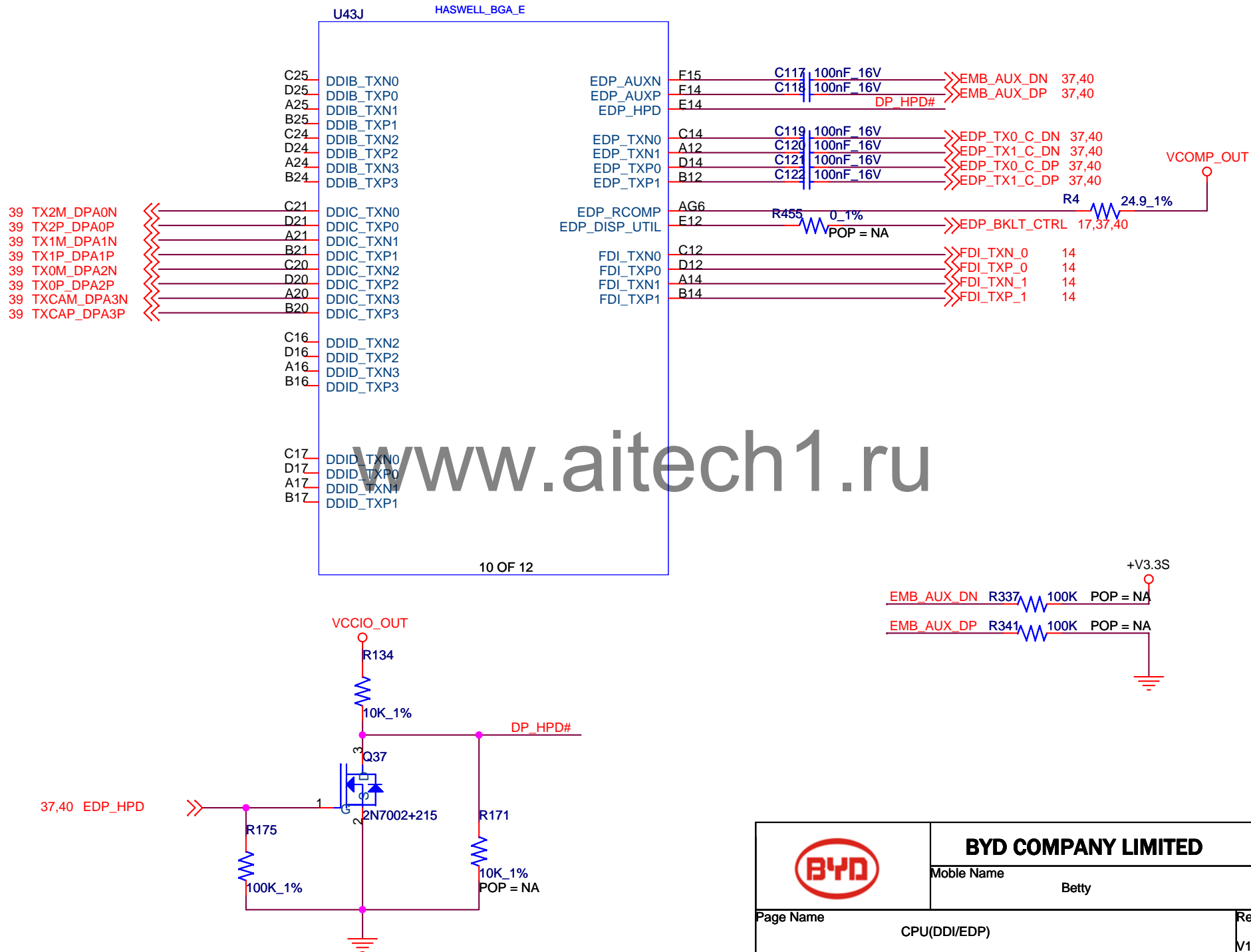
when ssc clock is not used, stuff them











BYD COMPANY LIMITED

Mobile Name

Betty

Page Name

CPU(DDI/EDP)

Rev

V1.0

Date: Sunday, May 05, 2013

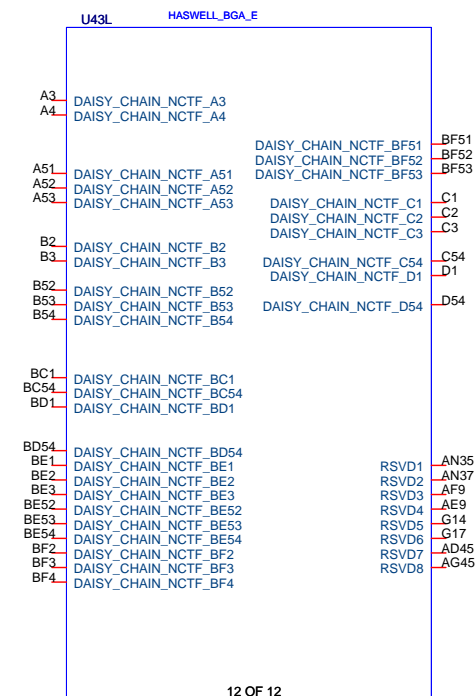
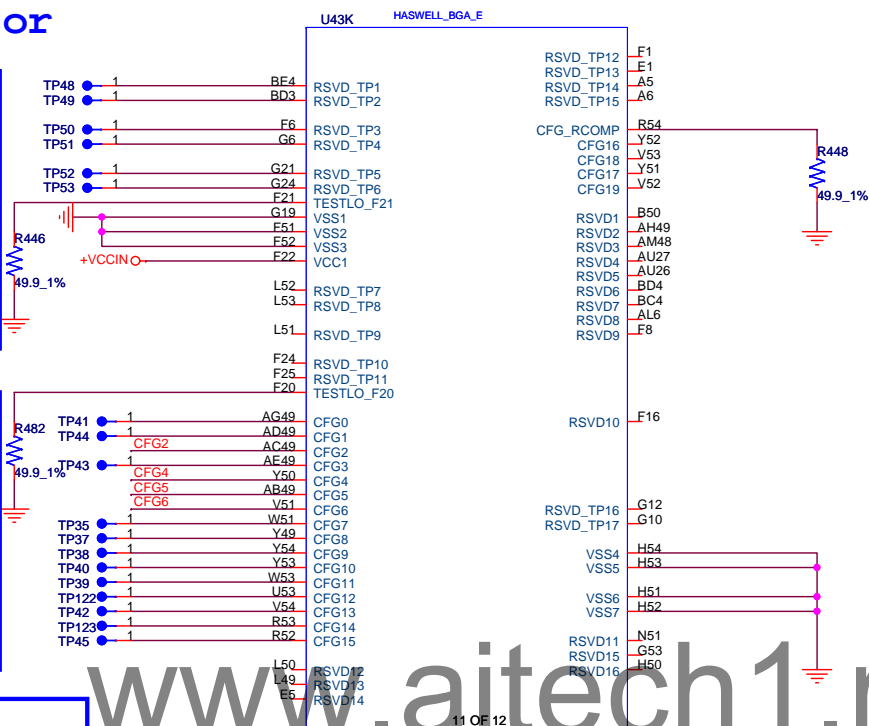
Sheet 7 of 51

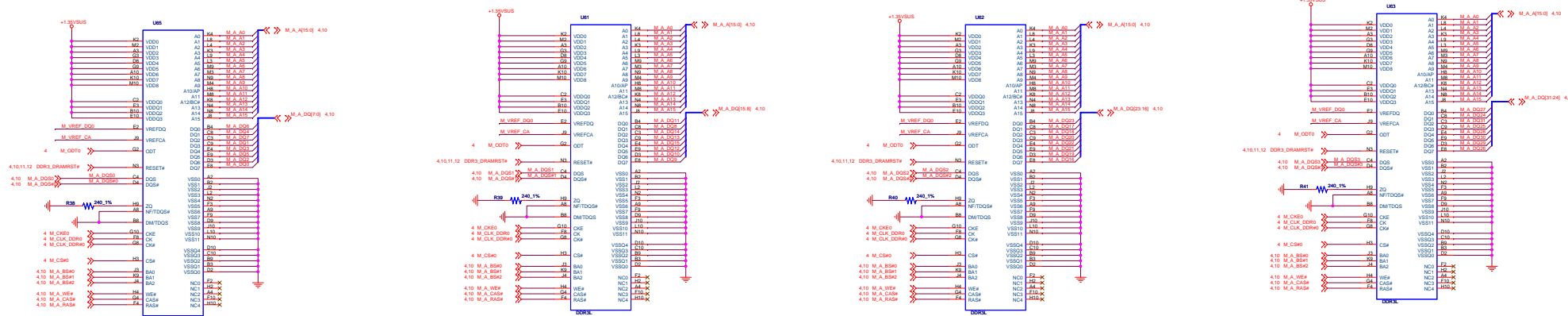
PEG Static Lane Reversal - CFG2 is for the 16x
1:(Default) Normal Operation; Lane #
definition matches socket pin map definition
0:Lane Reversed

The diagram shows a circuit for the CFG2 pin. A red oval encloses the components. At the top, a red line labeled 'CFG2' connects to a resistor labeled 'R416'. The resistor is represented by a blue zigzag line and is labeled '1K_1%' below it. To the right of the resistor, the text 'POP = NA' is written. The bottom of the resistor is connected to a ground symbol, which consists of three horizontal lines of decreasing width.

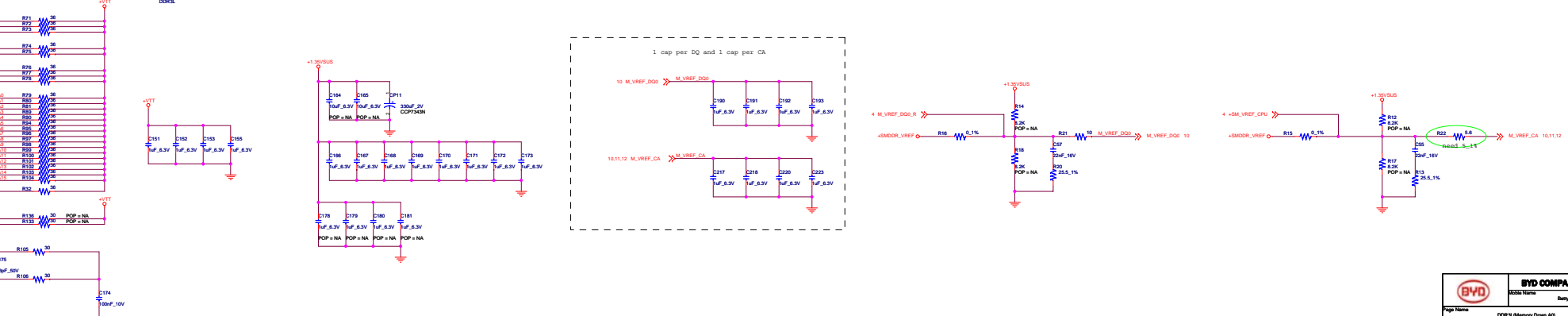
A circuit diagram showing a pull-up resistor R416. The resistor is connected between the CFG2 pin and ground. The resistor value is 1K_1% and its power-on-population (POP) is NA. The entire circuit is enclosed in a red oval.

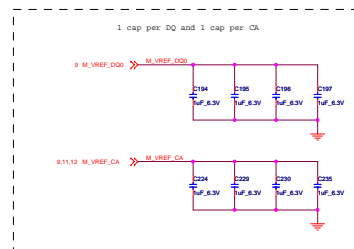
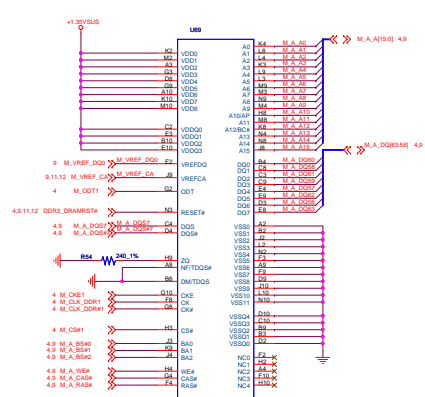
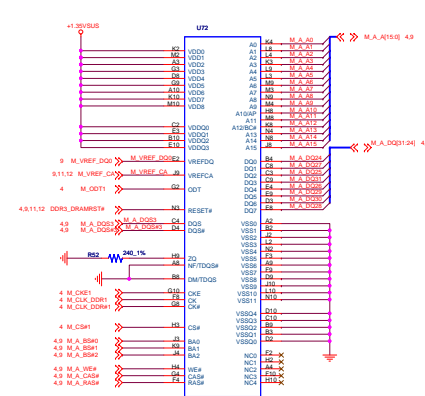
A circuit diagram showing a resistor labeled R415 with a value of 1K_1%. The resistor is connected between the CFG4 pin and ground.

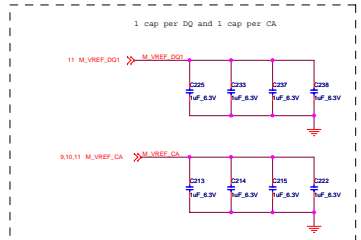
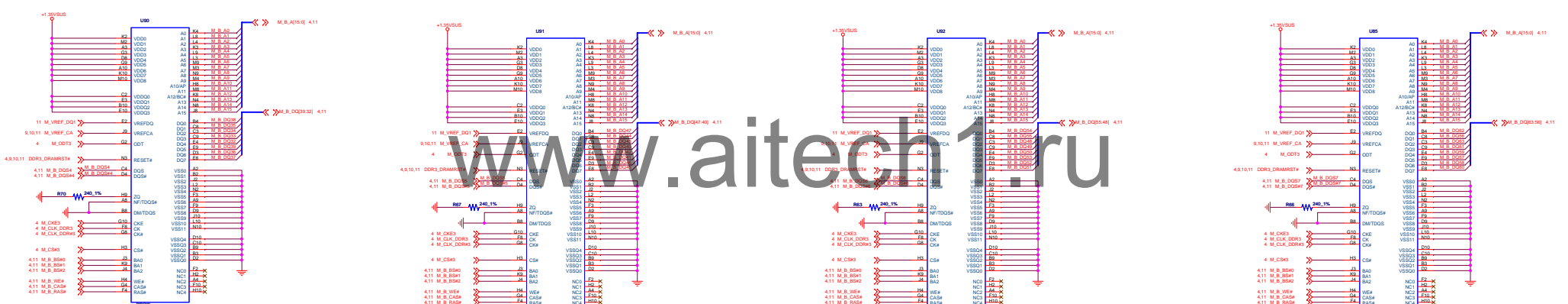
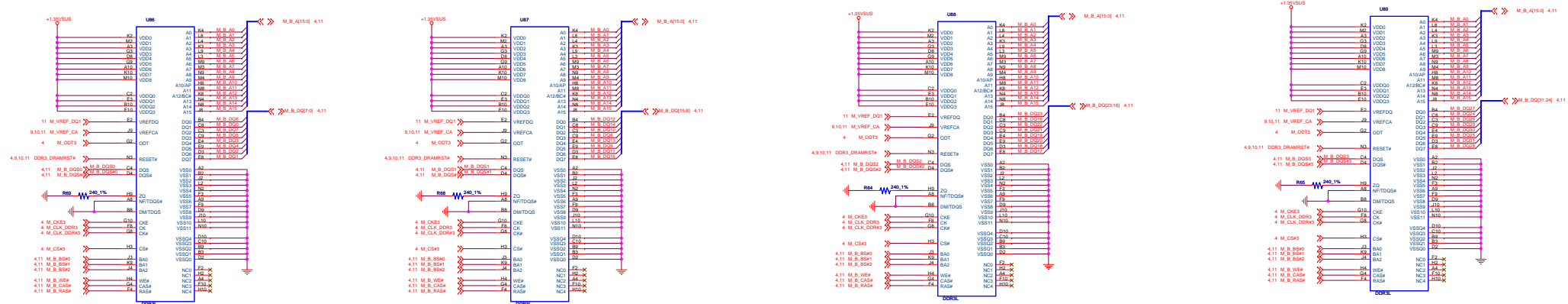


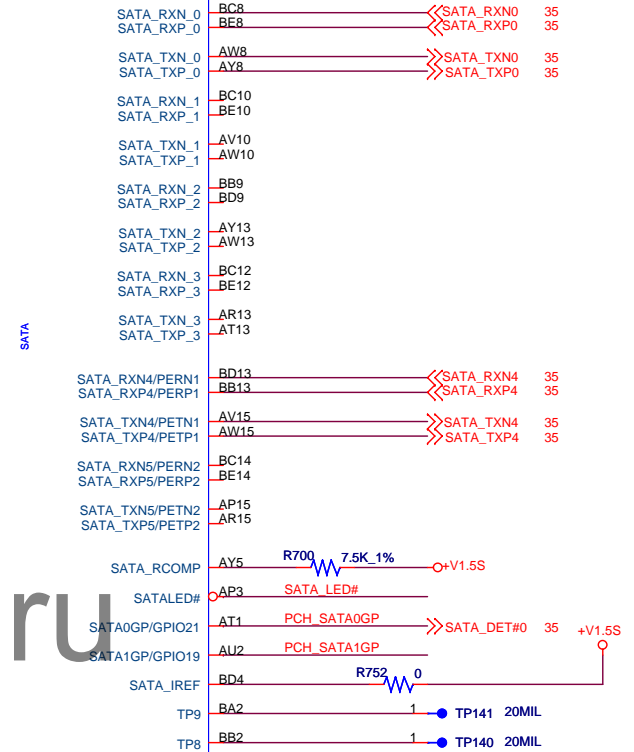
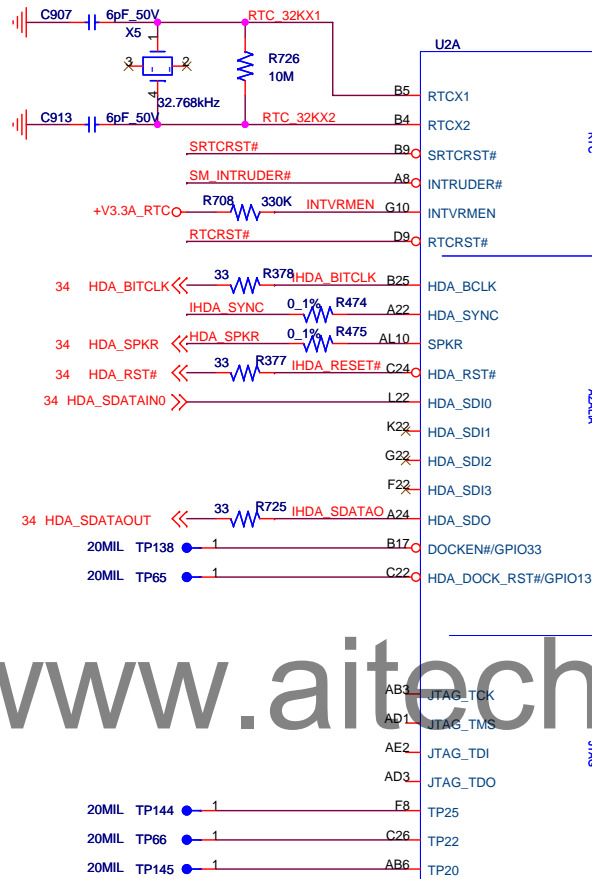
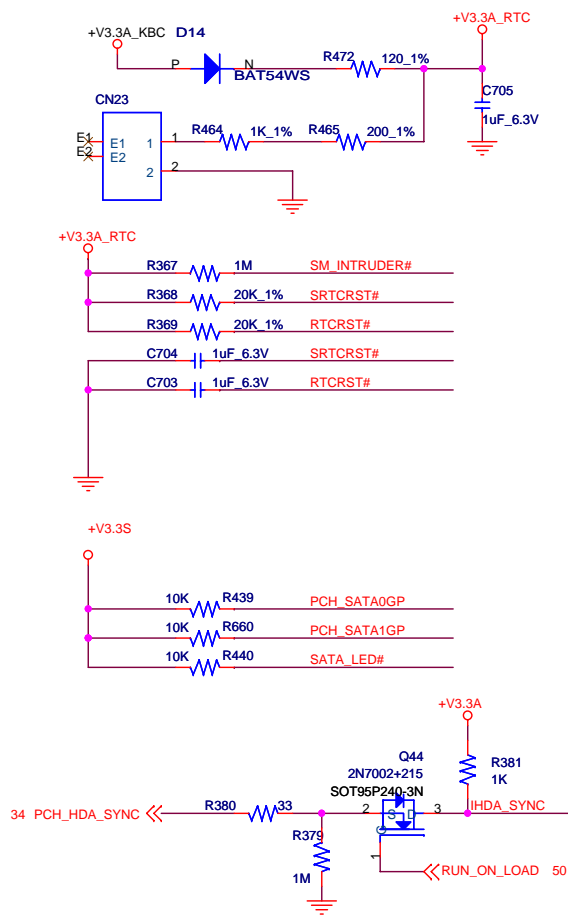


www.aitech.ru

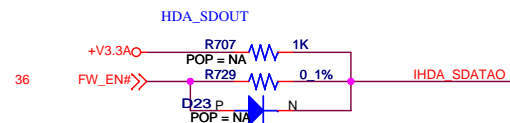


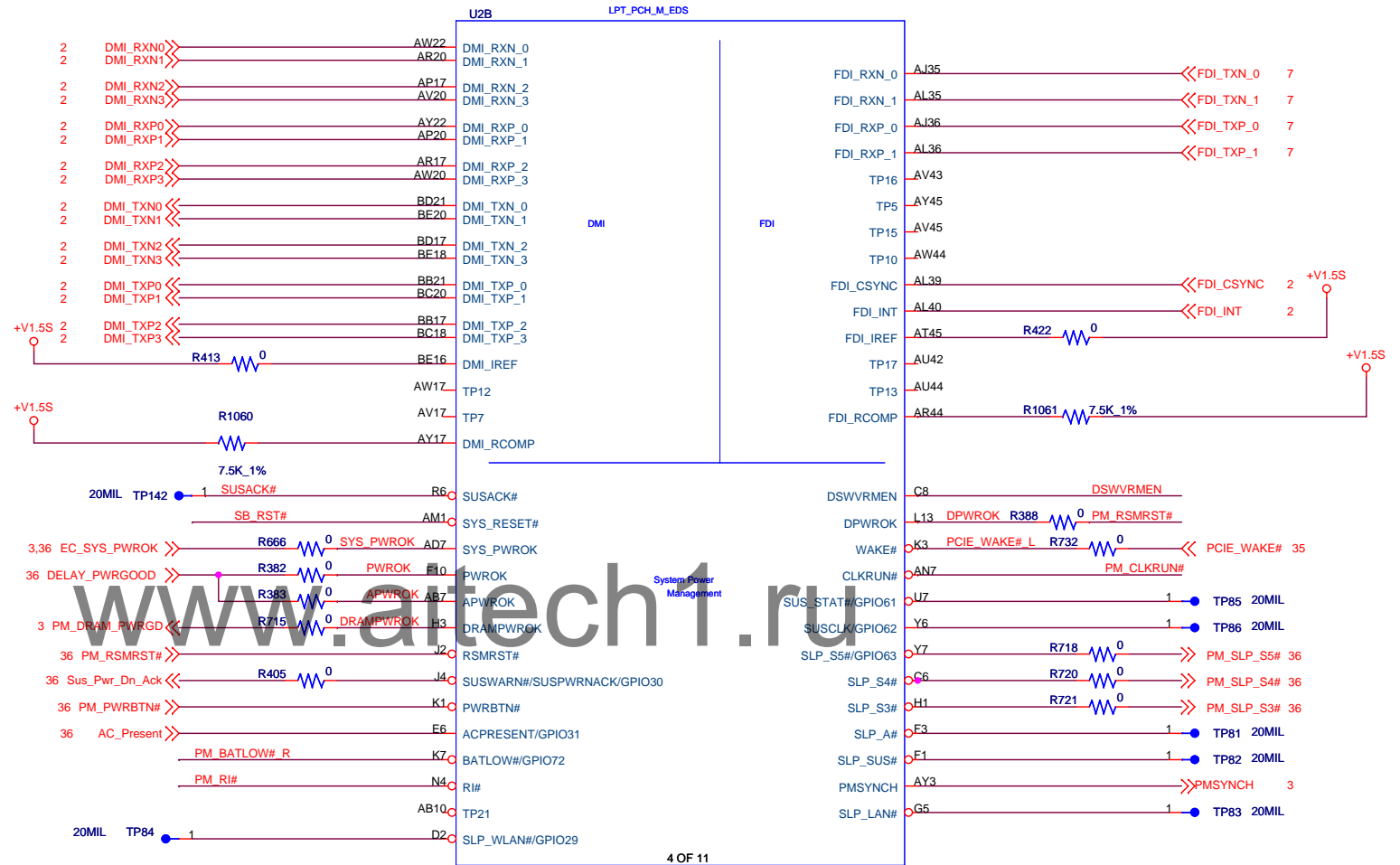
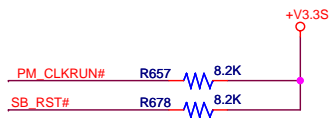
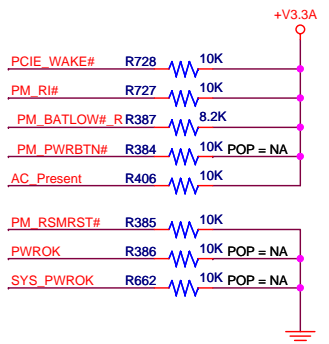
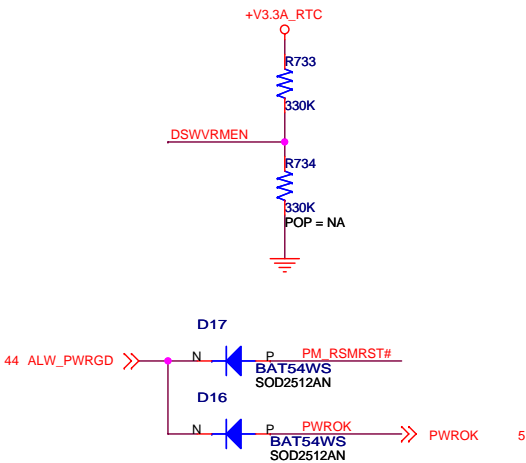


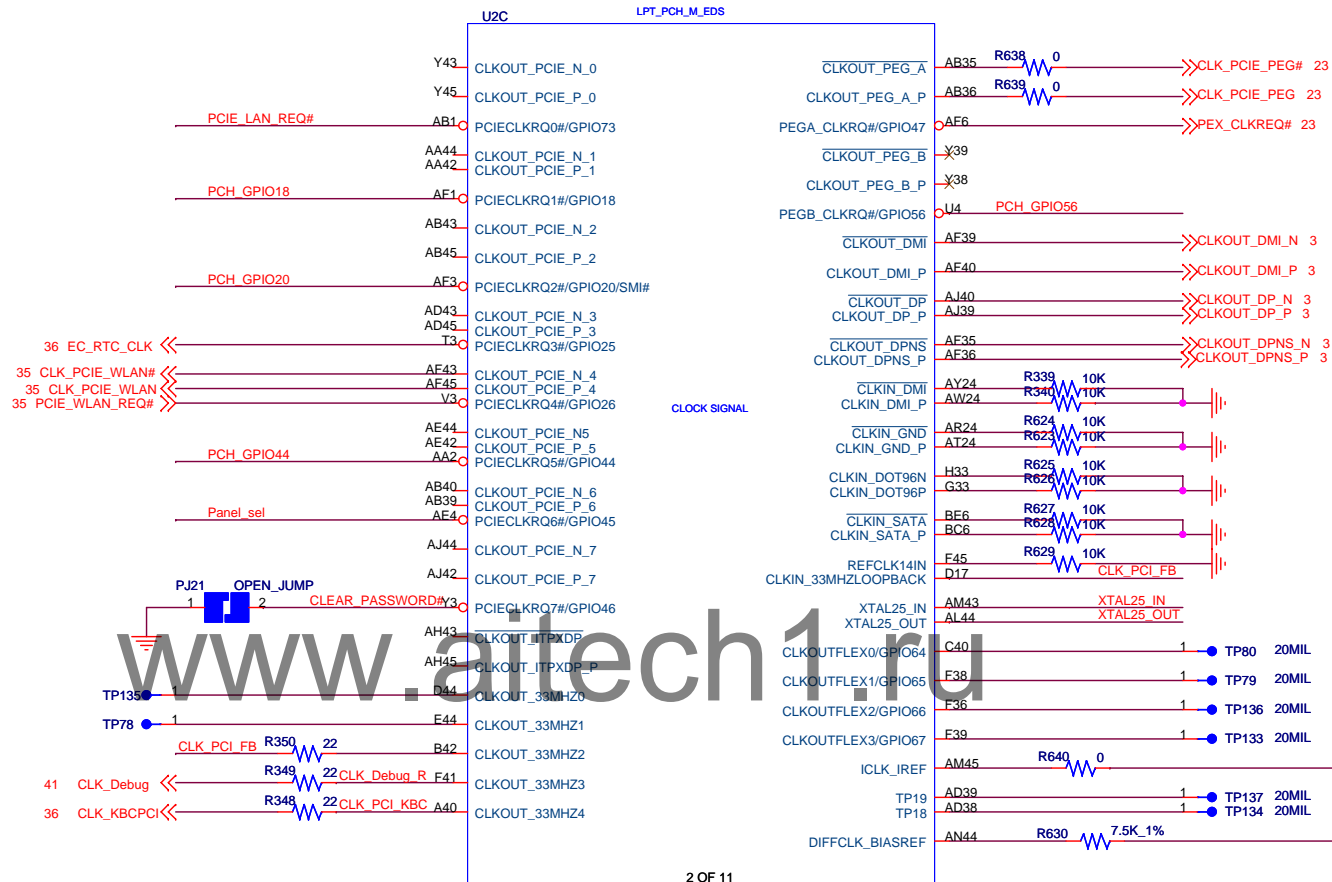
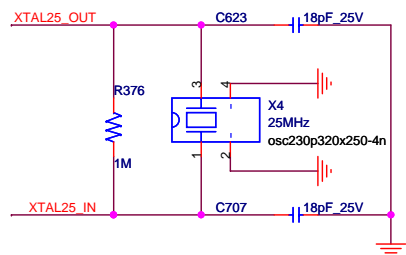
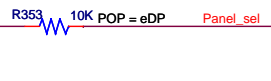
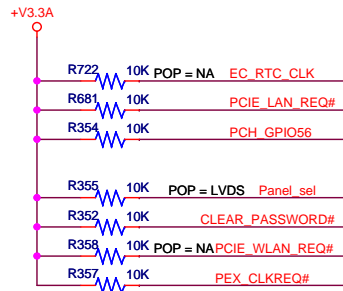
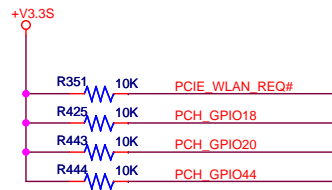




www.aitech1.ru







36 EC_RTC_CLK <<<

35 CLK_PCIE_WLAN# <<<

35 CLK_PCIE_WLAN# <<<

35 PCIE_WLAN_REQ# <<<

41 CLK_Debug <<<

36 CLK_KBCPCI <<<


PJ21 OPEN_JUMP

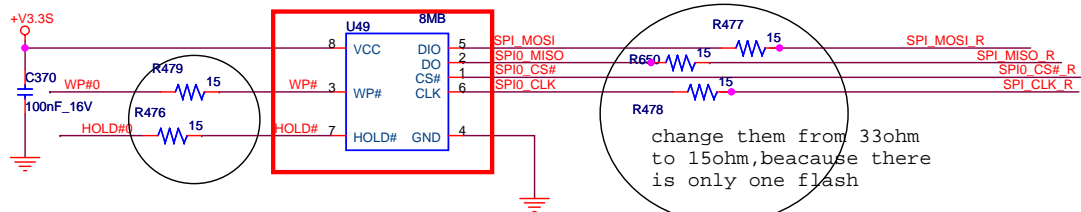
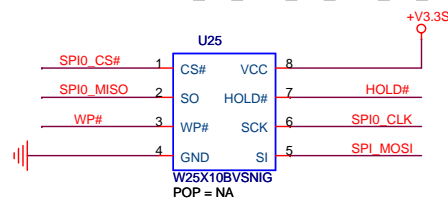
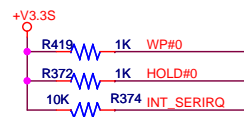
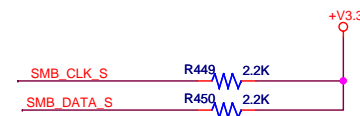
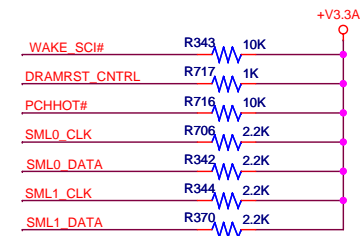
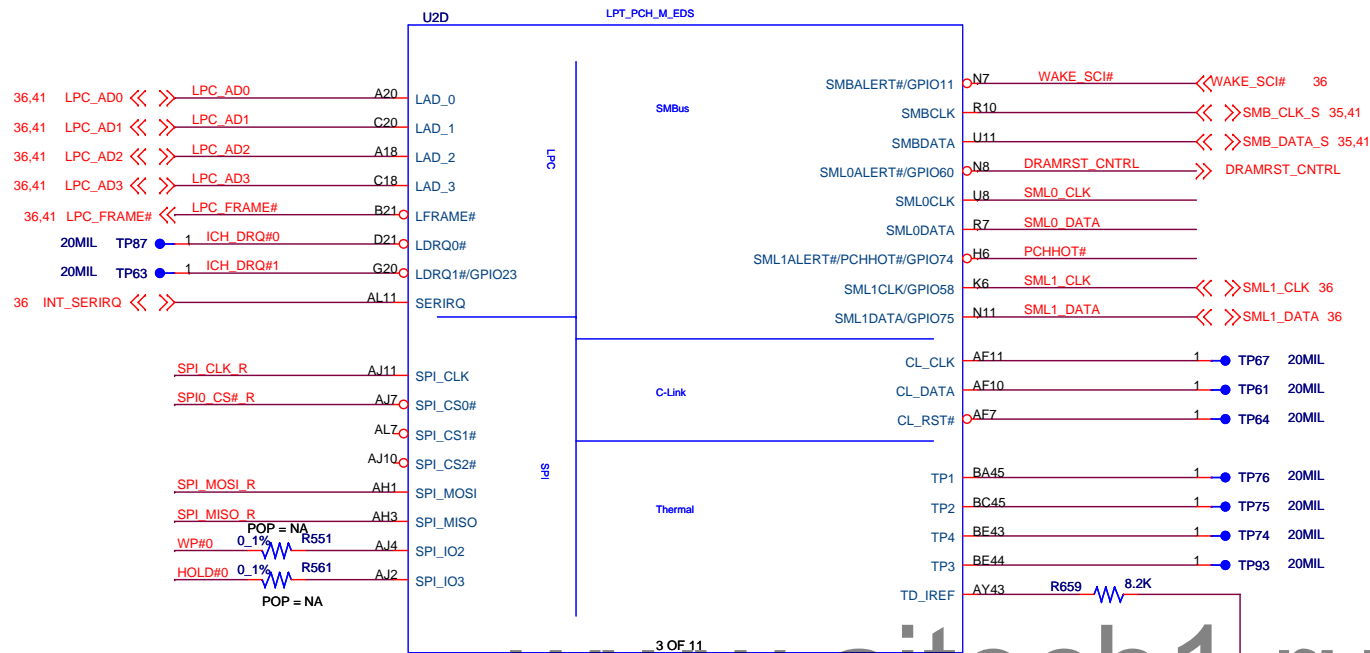
1 2 CLEAR_PASSWORD#

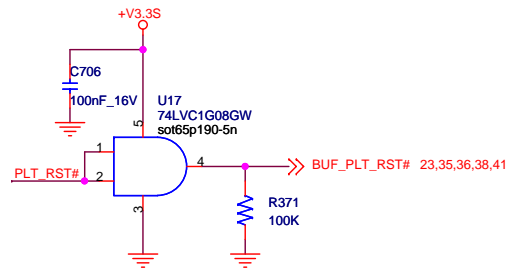
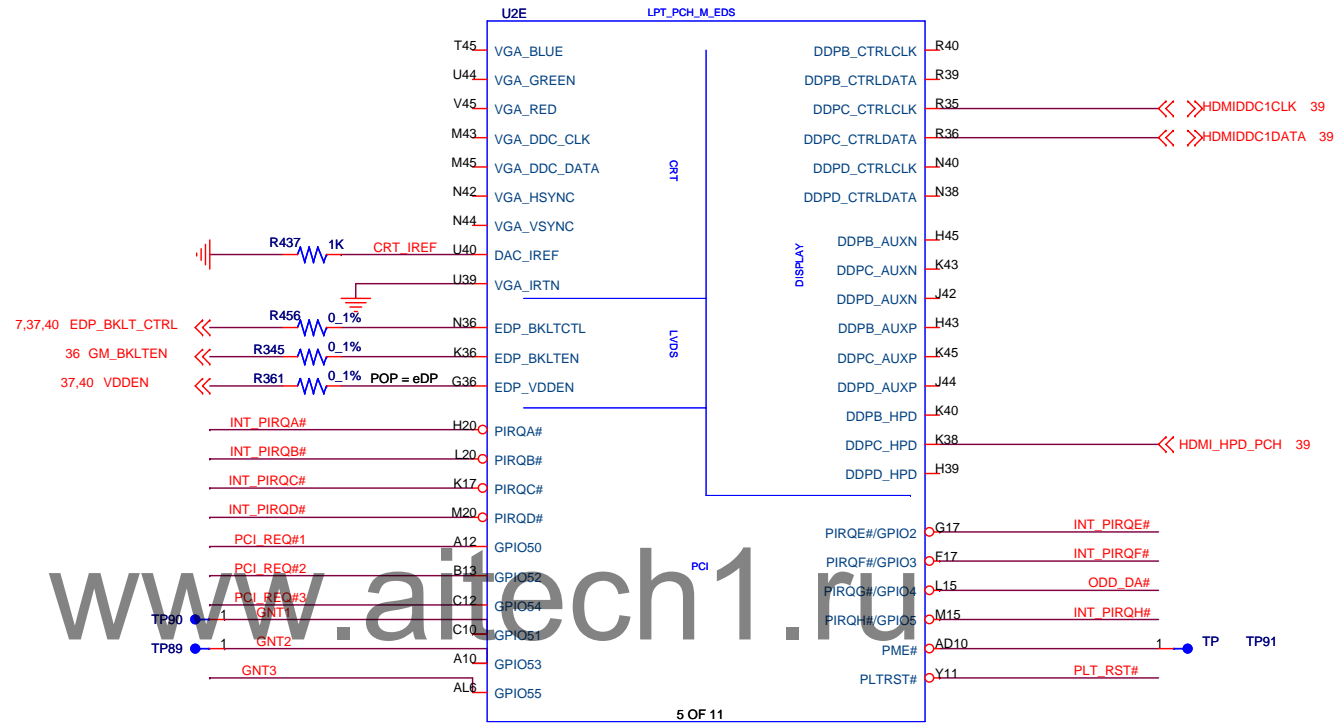
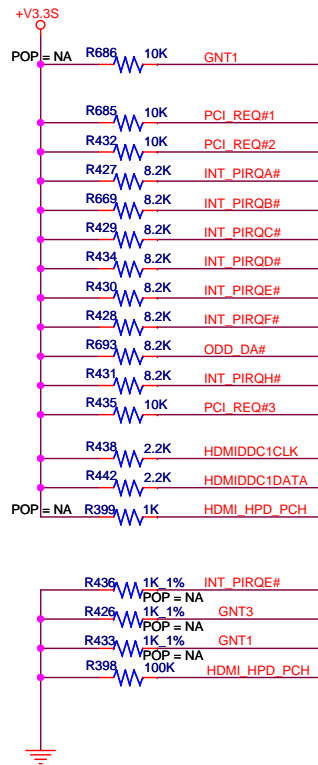
CLK_PCI_FB R350 22

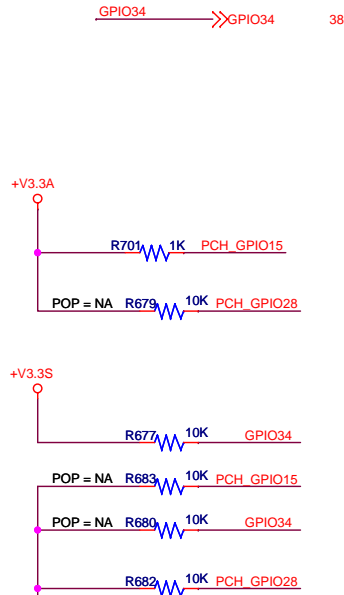
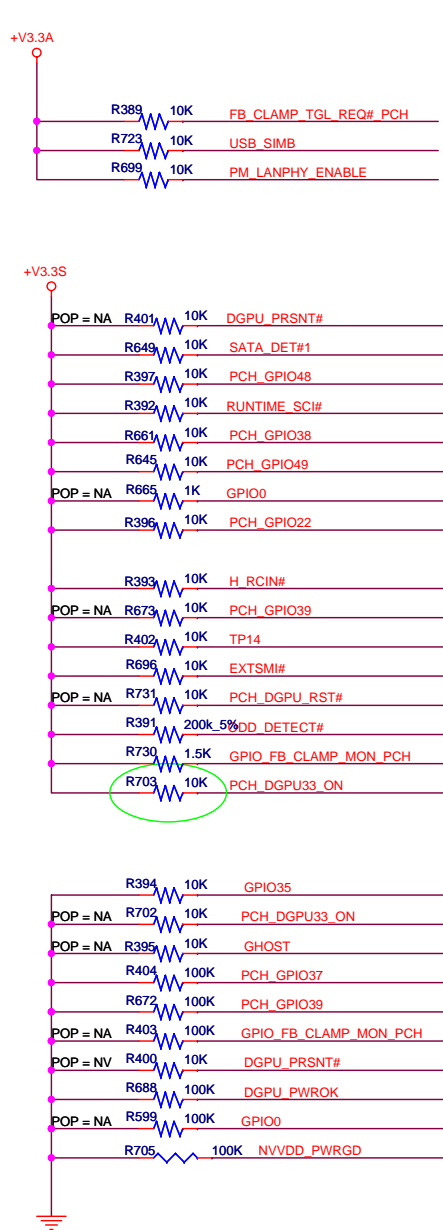
CLK_Debug_R R348 22

CLK_PCI_KBC R348 22

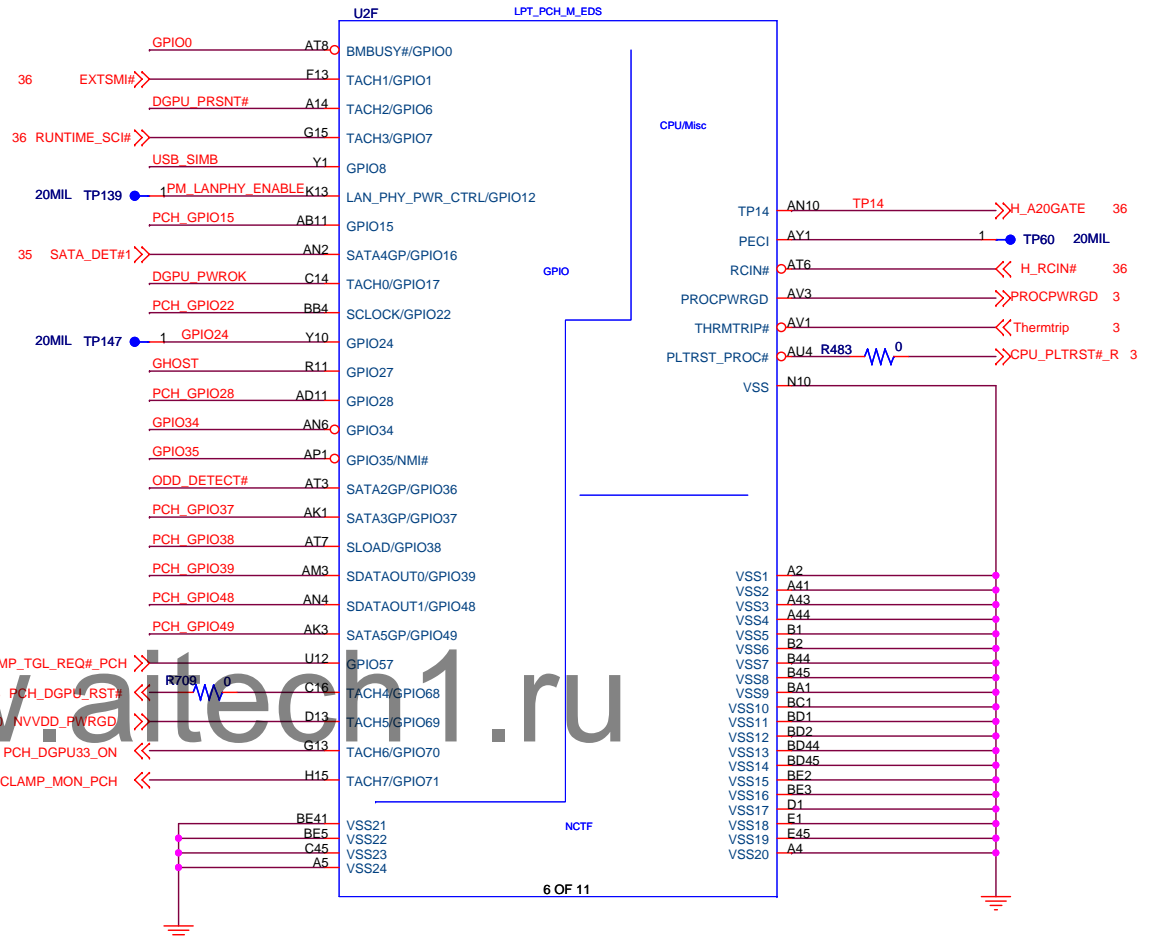
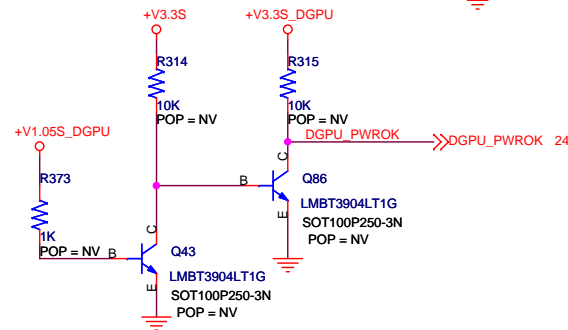
	BYD COMPANY LIMITED	
	Moble Name Betty	
Page Name	PCH(CLOCK SIGNALS)	Rev V1.0
Date: Sunday, May 05, 2013	Sheet 15	of 51

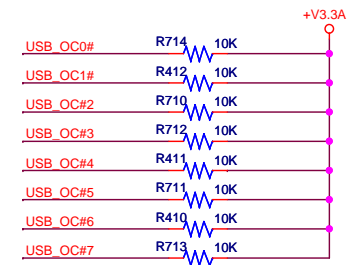


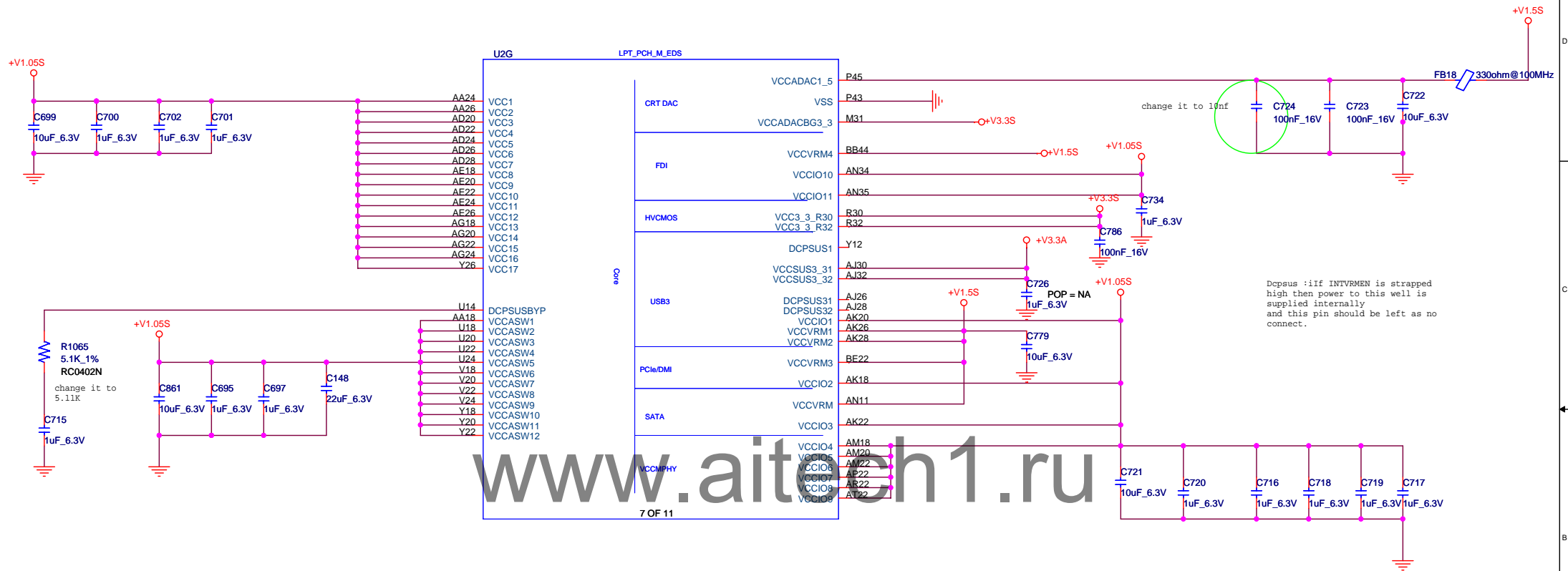




www.aitech1.ru

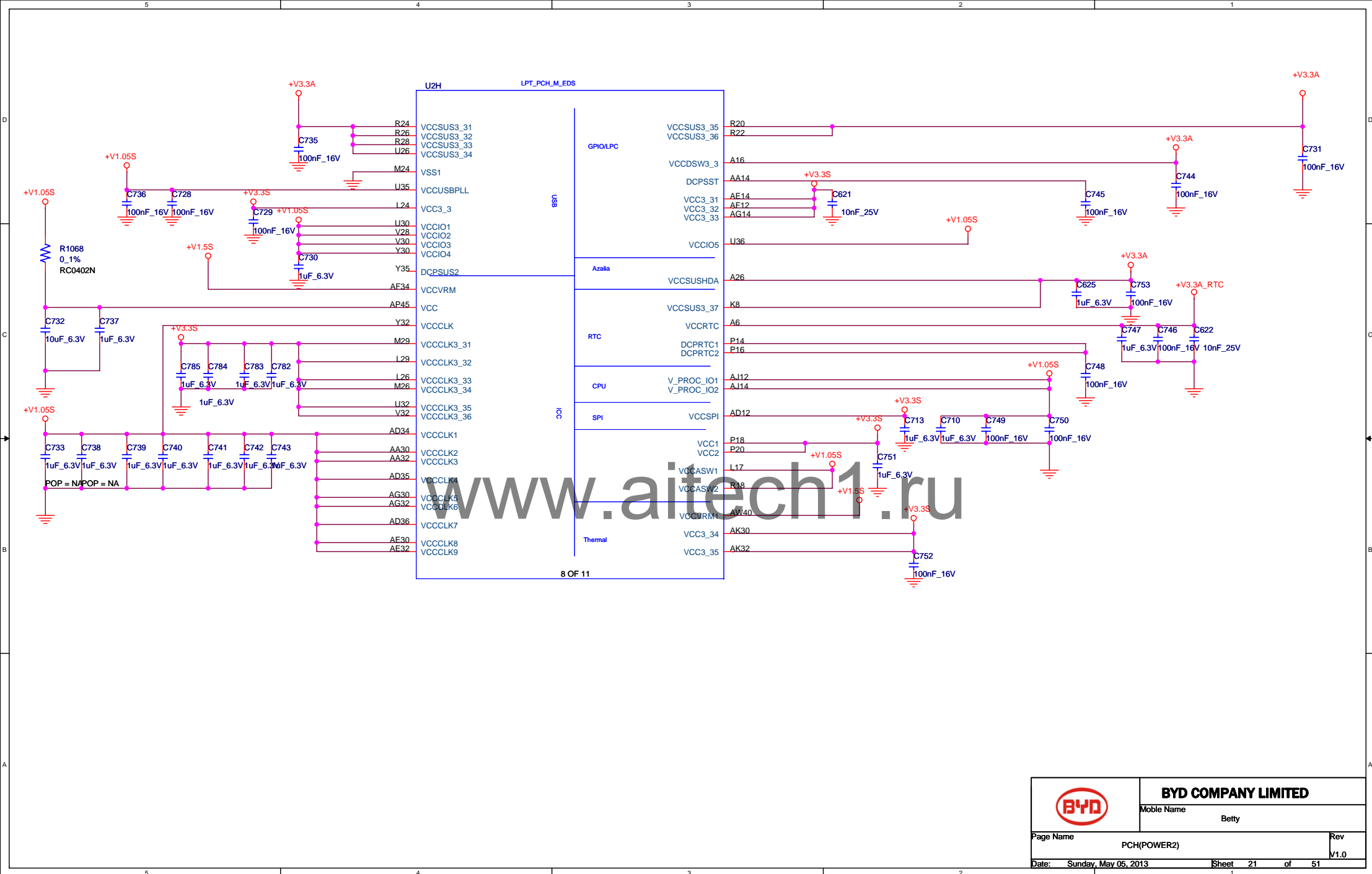


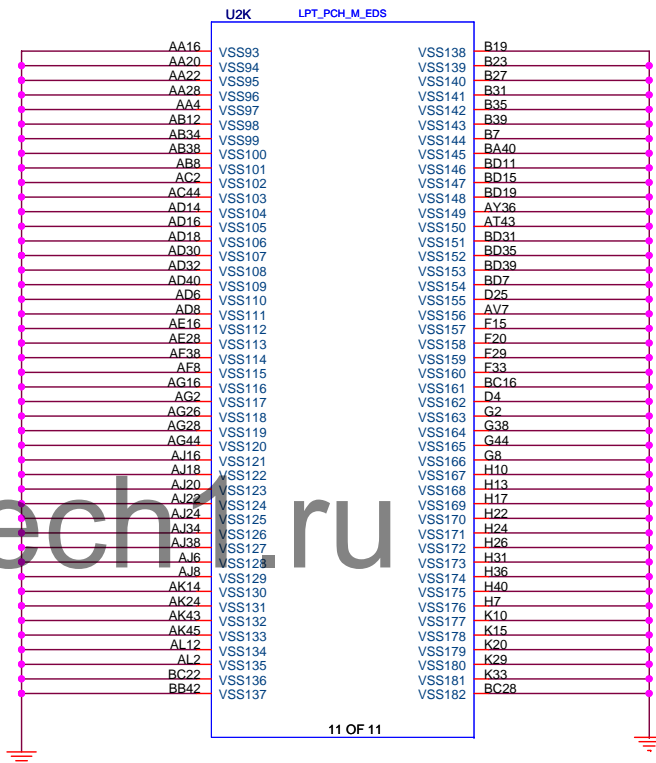
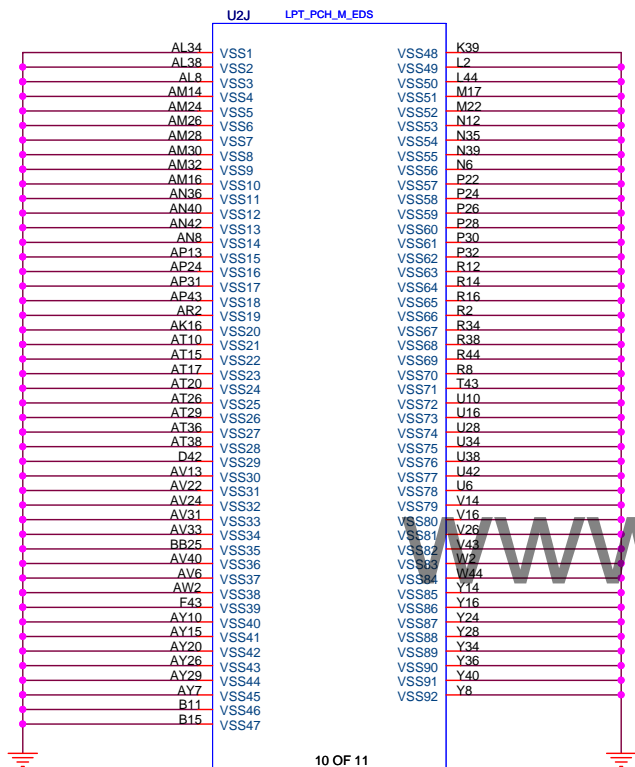


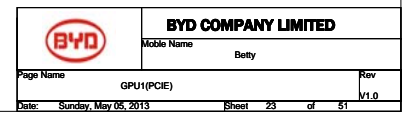


www.aitch1.ru

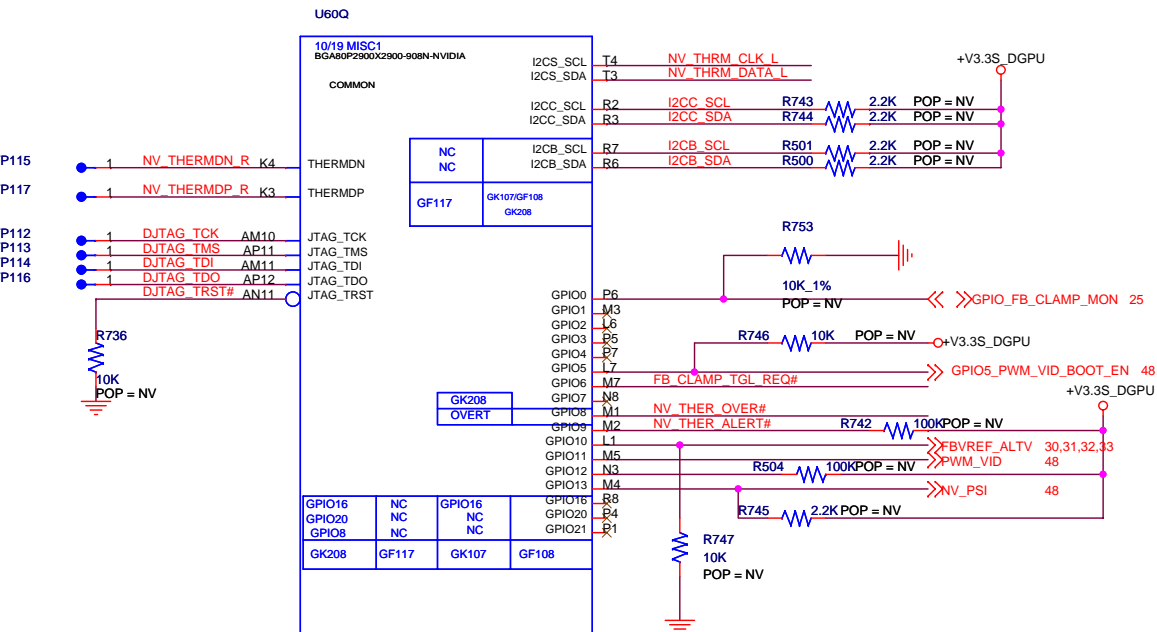
	BYD COMPANY LIMITED	
	Moble Name	Betty
Page Name	PCH(POWER1)	Rev V1.0
Date: Sunday, May 05, 2013	Sheet 20	of 51



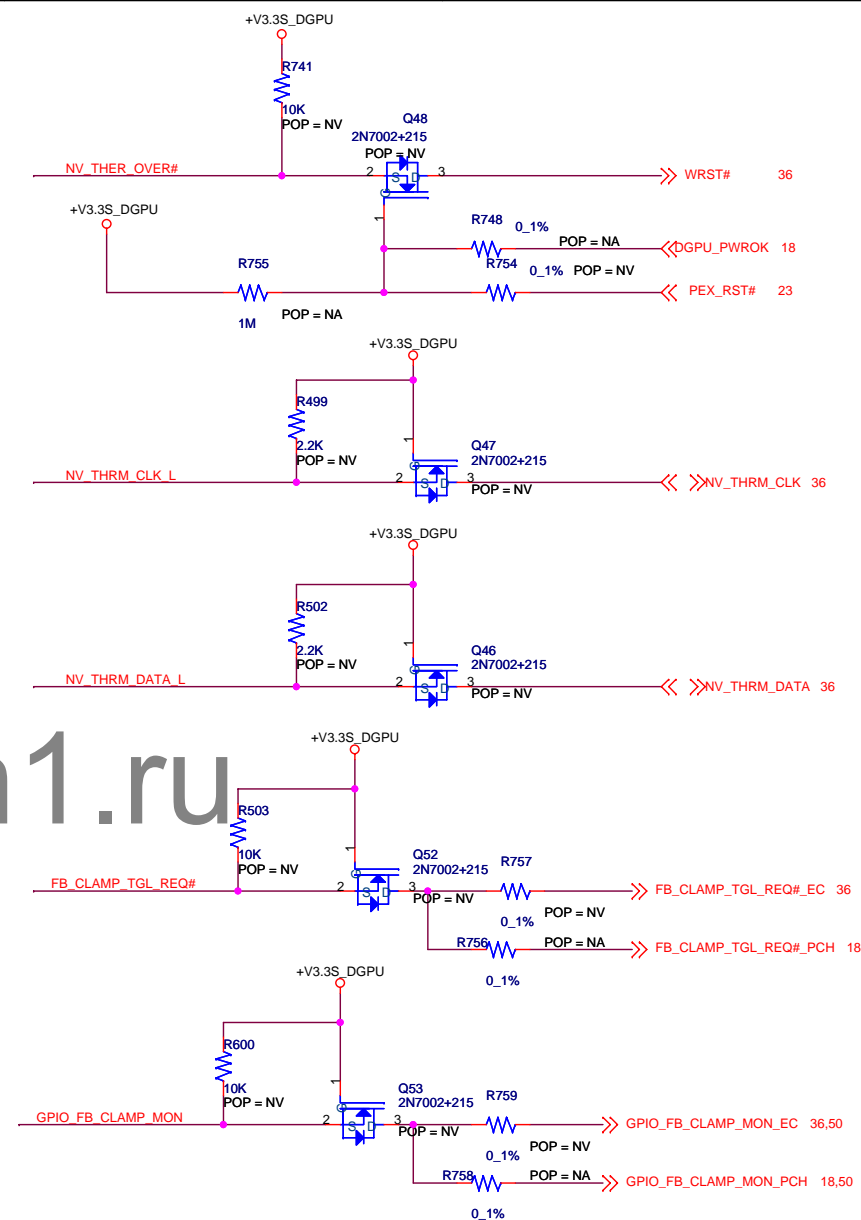





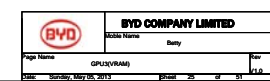
www.aitech1.ru

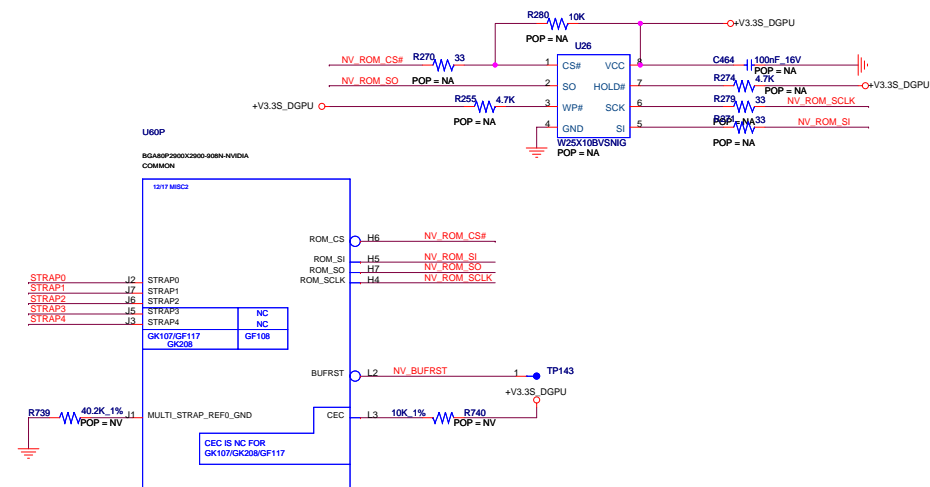


GPIO	Function
GPIO 0	FB_CLAMP_MON
GPIO 1	MEM_VDD_CTL
GPIO 2	LCD_BL_PWM
GPIO 3	LCD_VCC
GPIO 4	LCD_BLEN
GPIO 5	Reserved
GPIO 6	FB_CLAMP_TGL_REG
GPIO 7	3DVision
GPIO 8	OVERT
GPIO 9	ALERT
GPIO 10	MEM_VREF_CTL
GPIO 11	PWM_VID
GPIO 12	PWR_Level
GPIO 13	PSI
GPIO 14	HPD_A
GPIO 15	HPD_C
GPIO 16	FRM_LCK
GPIO 17	HPD_D
GPIO 18	HPD_E
GPIO 19	HPD_F or HPD_B
GPIO 20	Reserved
GPIO 21	Reserved



	BYD COMPANY LIMITED	
	Moble Name Betty	
Page Name GPU2(GPIO)		Rev V1.0
Date: Sunday, May 05, 2013		Sheet 24 of 51



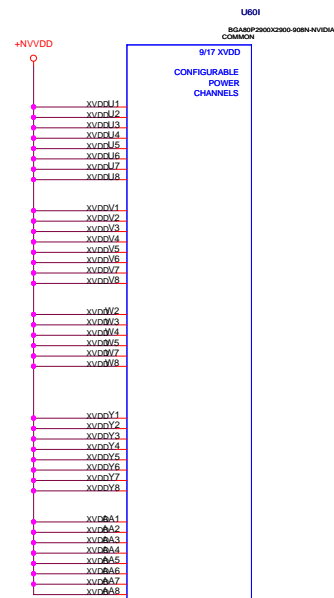


The schematic diagram illustrates the power supply section of the STM32F405RG microcontroller. It features a 3.3V regulator (R510) connected to a 3.3V input (V3.3S_DGPU) and a 3.3V output (V3.3S_3.3V). The regulator is connected to the VDD and VDDA pins of the microcontroller. The schematic also shows the connection of the microcontroller's pins to the power supply rails. The microcontroller is shown in a simplified block diagram with pins labeled VDD, VDDA, and VDDIO. The power supply rails are labeled V3.3S_3.3V and V3.3S_DGPU. The schematic is a simplified representation of the power supply section of the STM32F405RG microcontroller.

```
Memory:
Hynix      H5GQ2H24AFR-T2C
Samsung    K4G20325FD-FC04
```

GK208/107 MEM STRAP TABLE	
RAMCFG[3:0]	CONFIG
0100	128Mx16 GDDR5 1.5V HYNIX
0101	128Mx16 GDDR5 1.5V SAMSUNG

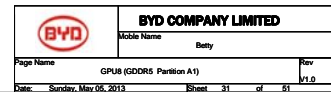
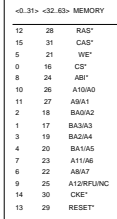
```
ROM_SI:
Hynix          H5GQ2H24AFR-T2C ==> R518=34.8K
Samsung       K4G20325FD-FC04 ==> R517=45.3K
```

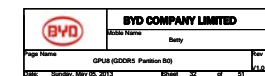


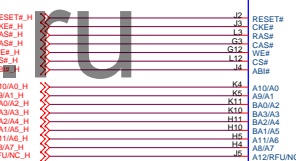
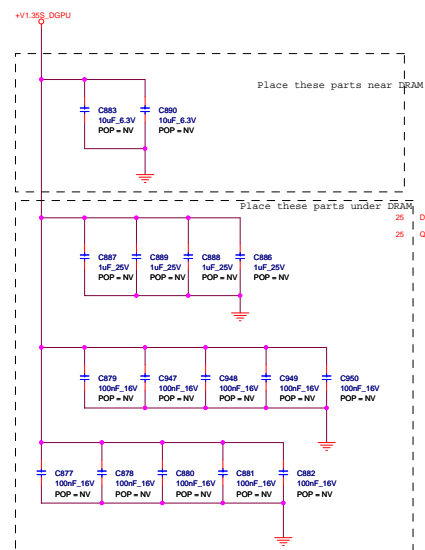
GDOR5 CMD Mapping Table

GDOR5 CMD Mapping Table
10 31+ -GDOR5 MEMORY
12 28 BA0P
15 31 C0P
5 21 WE
6 16 C0P
5 24 AB
10 25 A1000
11 27 BA0A
2 18 BA0A2
1 17 BA0A3
3 18 BA0A4
2 23 A1006
6 22 AB07
5 25 A1008FUNC
14 30 C0P
13 29 RESET

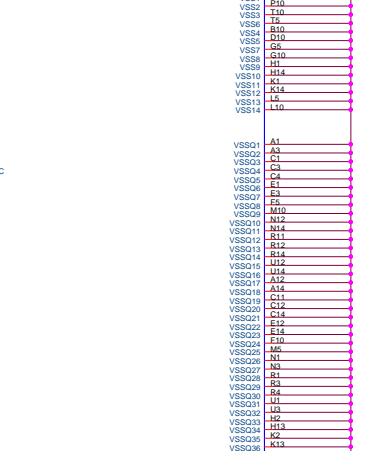
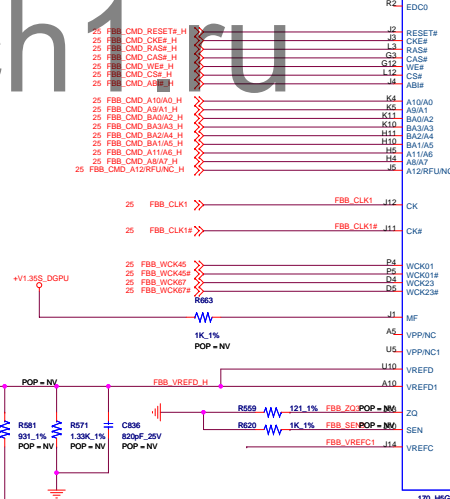
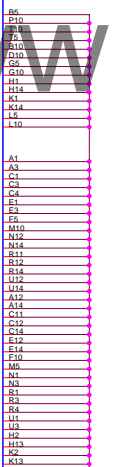
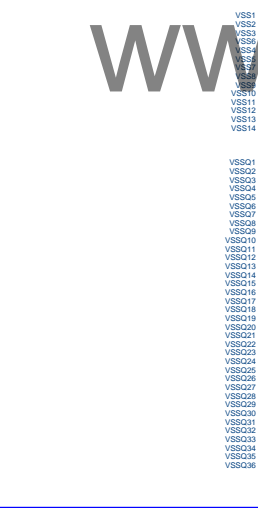








<0..31>	<32..63>	MEMORY
12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	AB1*
10	26	A10/A0
11	27	A9/A1
2	18	BA0/A2
1	17	BA3/A3
3	19	BA2/A4
4	20	BA1/A5
7	23	A11/A6
6	22	AS/A7
9	25	A12/R/UNCL
14	30	CKE*
13	29	RESET*



DIGITAL
(Include Thermal pad)

R318 47K R20402H <<HDA_SSPK 3

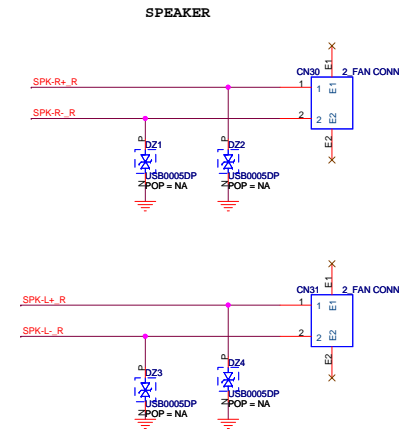
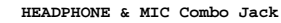
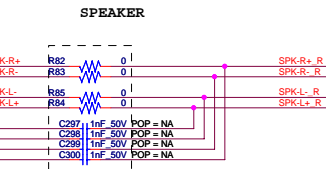
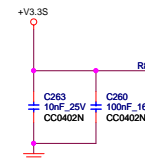
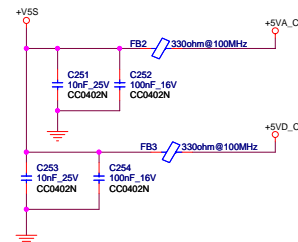
C276 1uF 16V

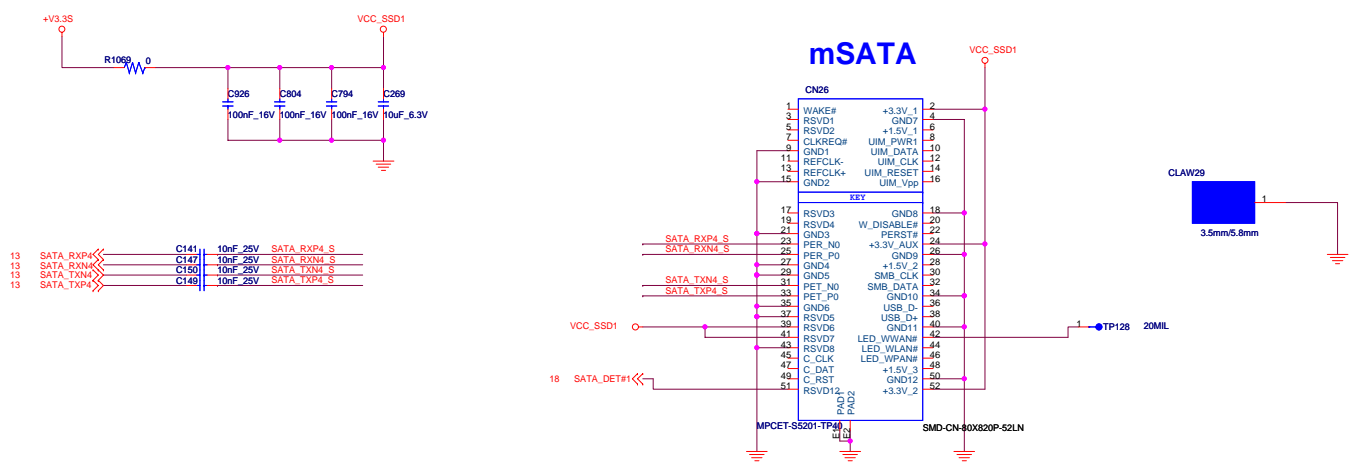
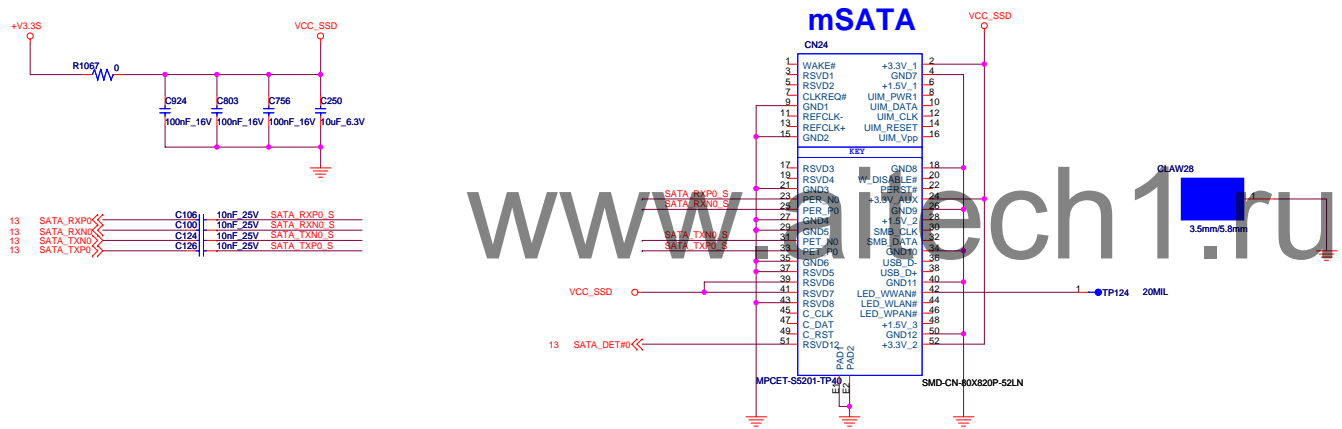
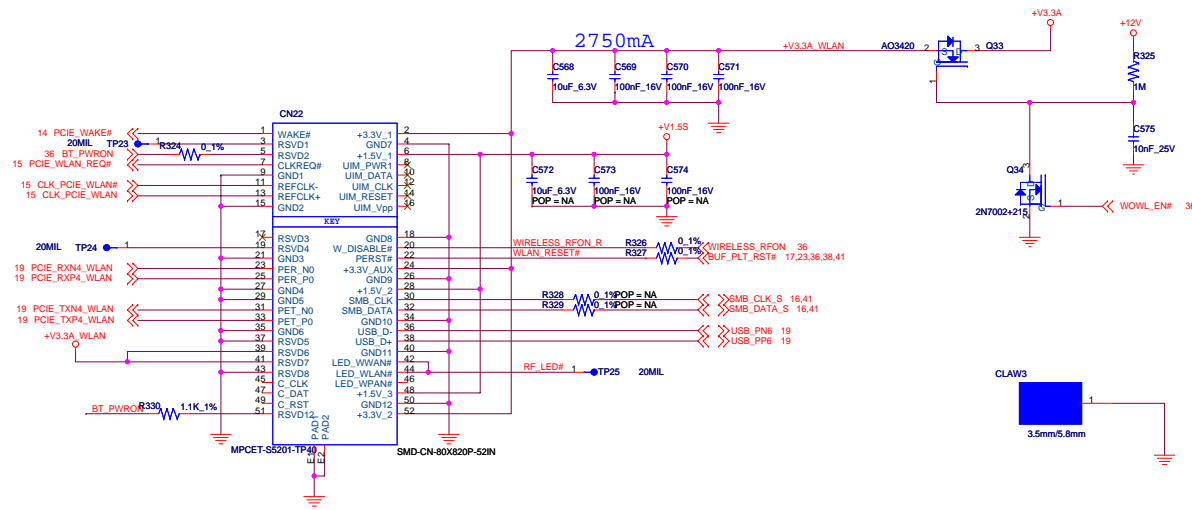
R331 4.7K

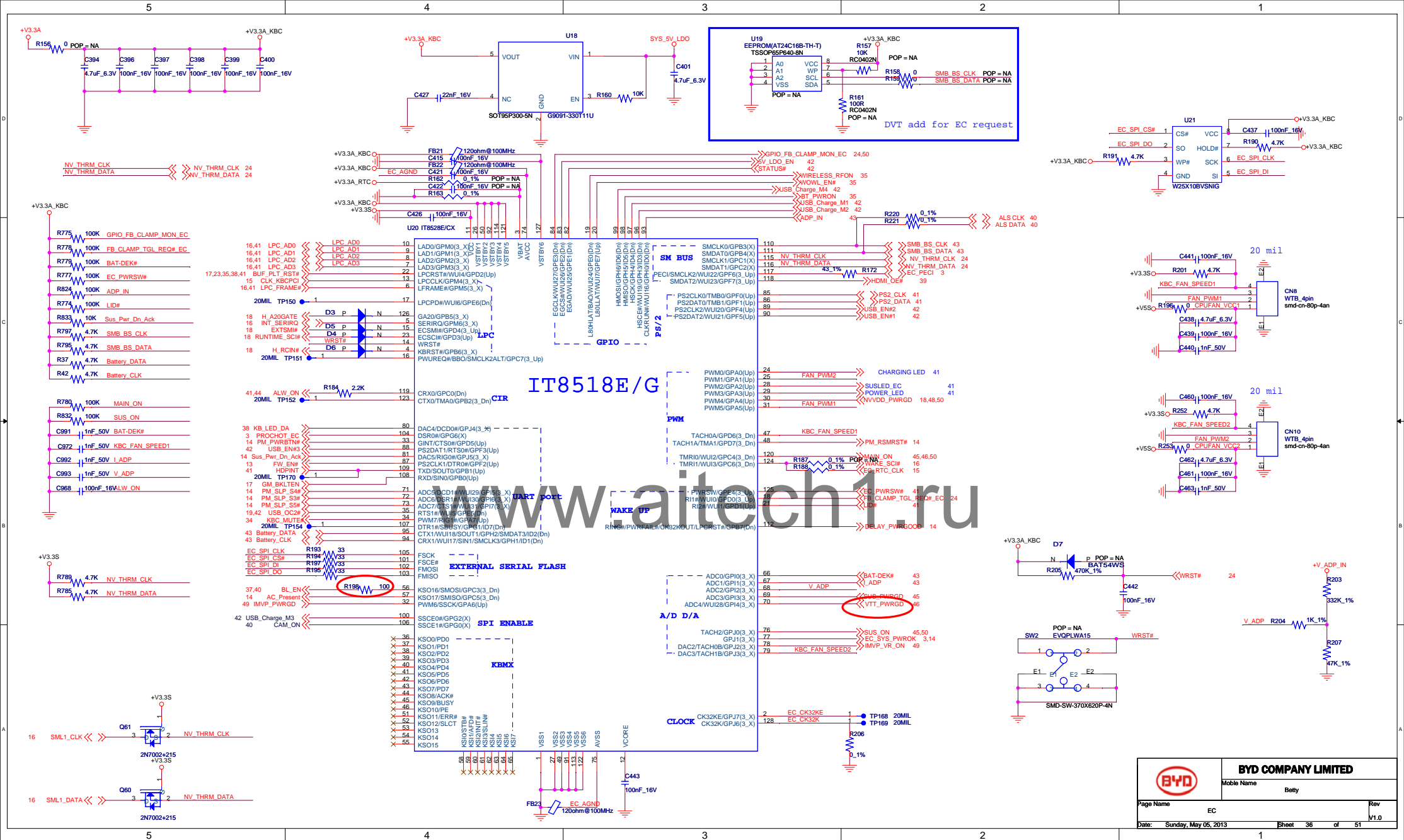
C277 100uF 50V

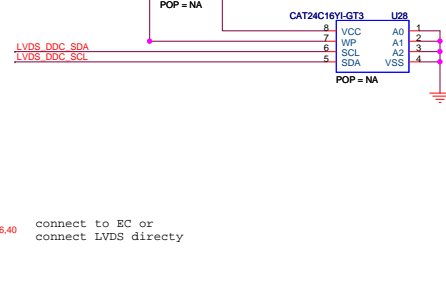
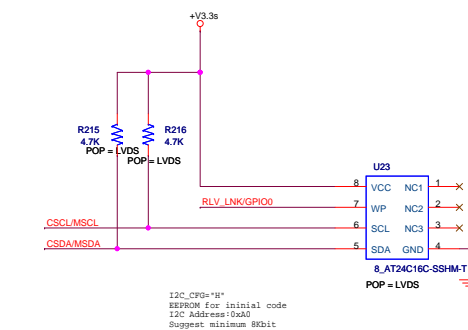
+3.3V0.C

PD#=0V : Power down Class D SPK amplifier
PD#=3.3V : Power up Class D SPK amplifier



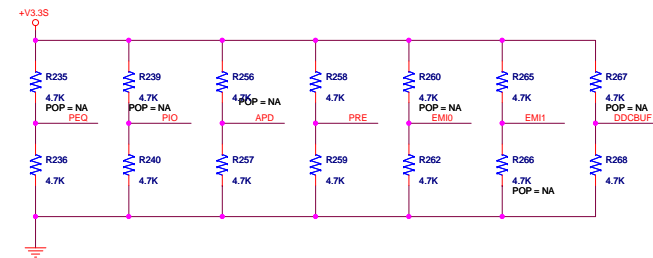
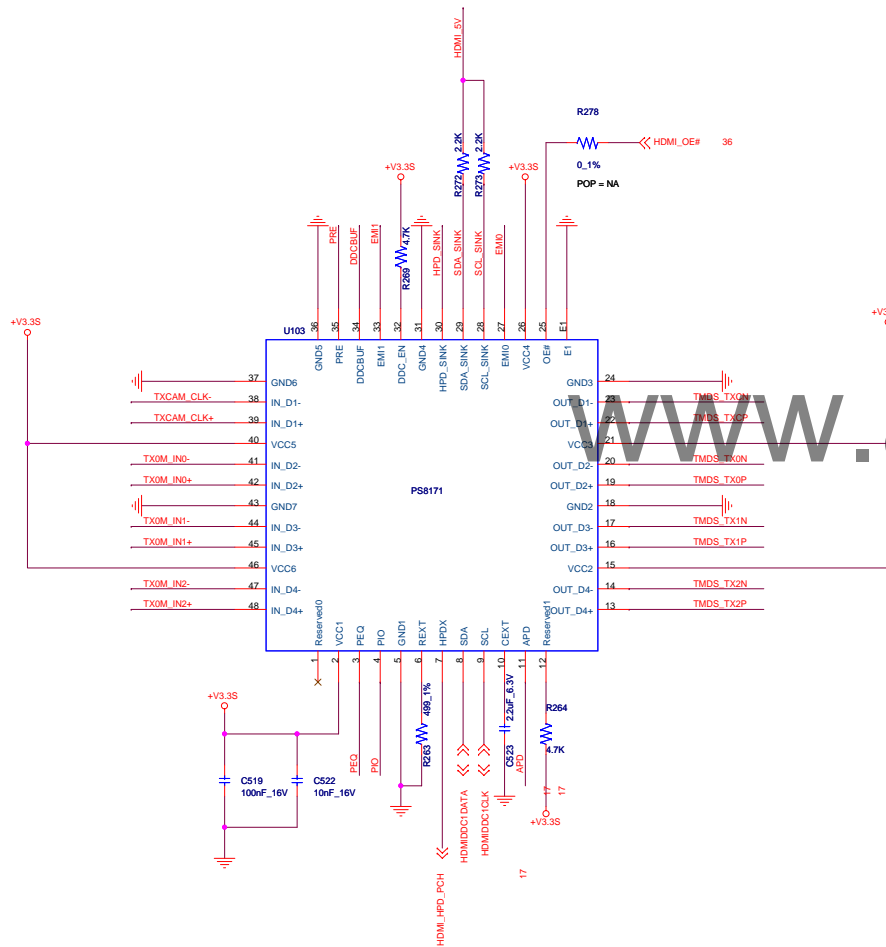
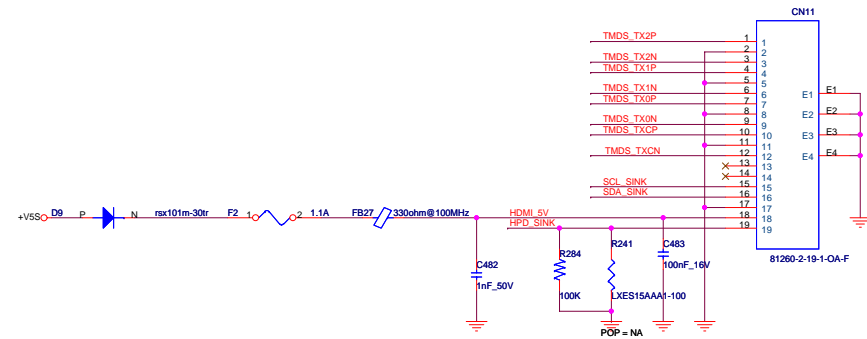


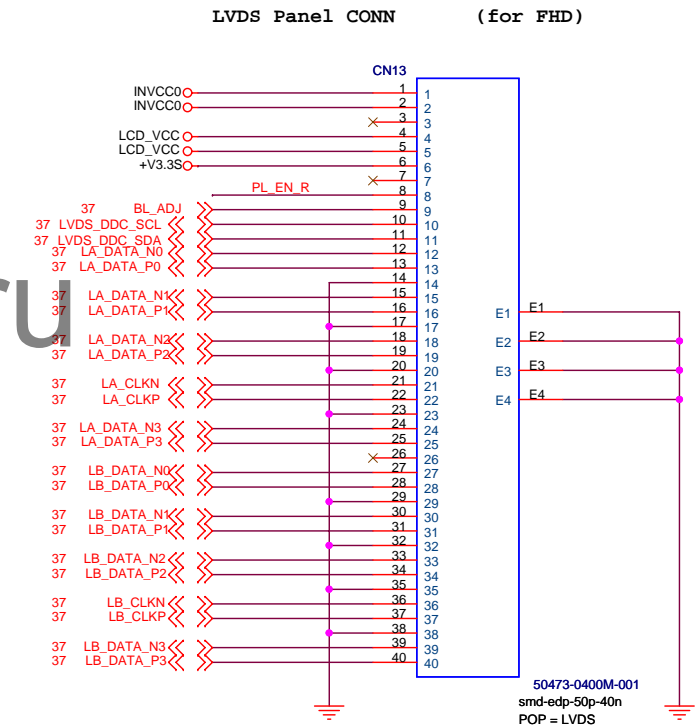
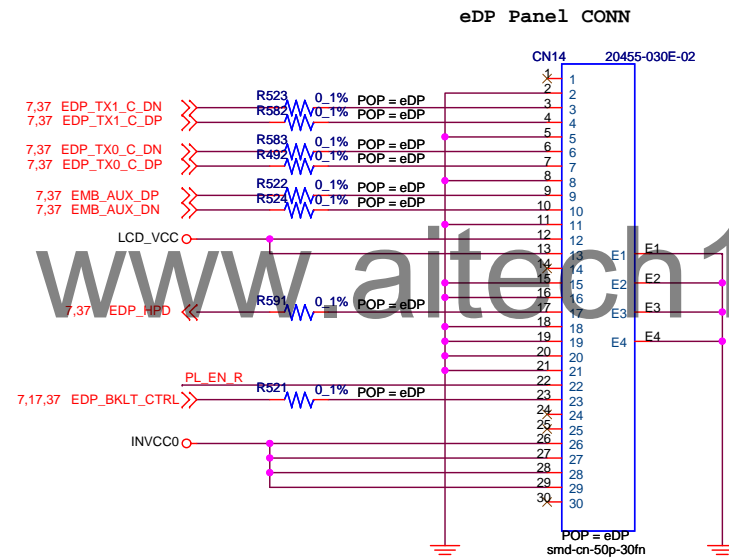
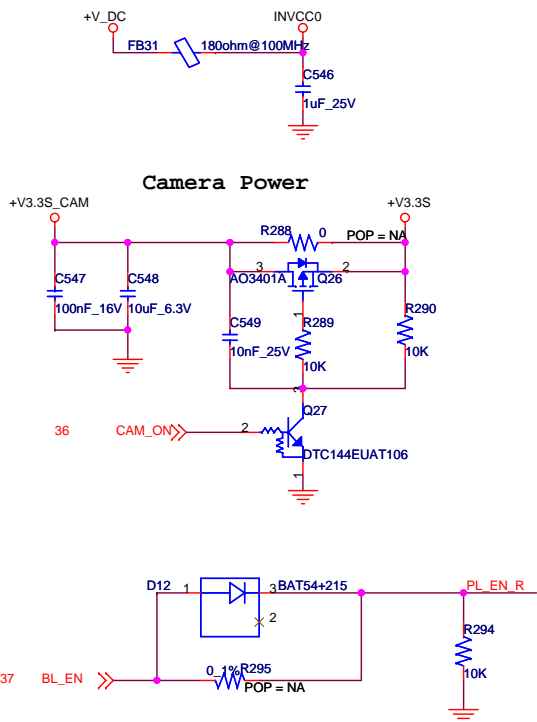
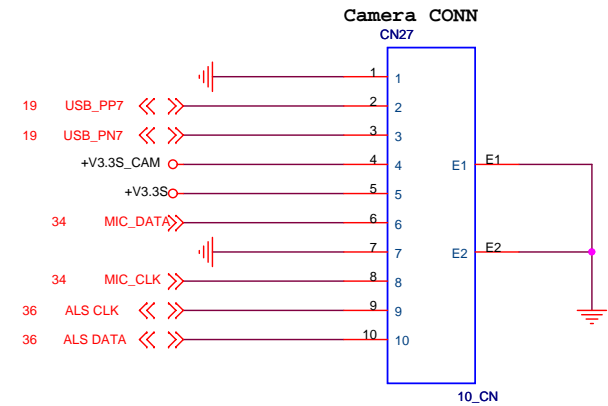
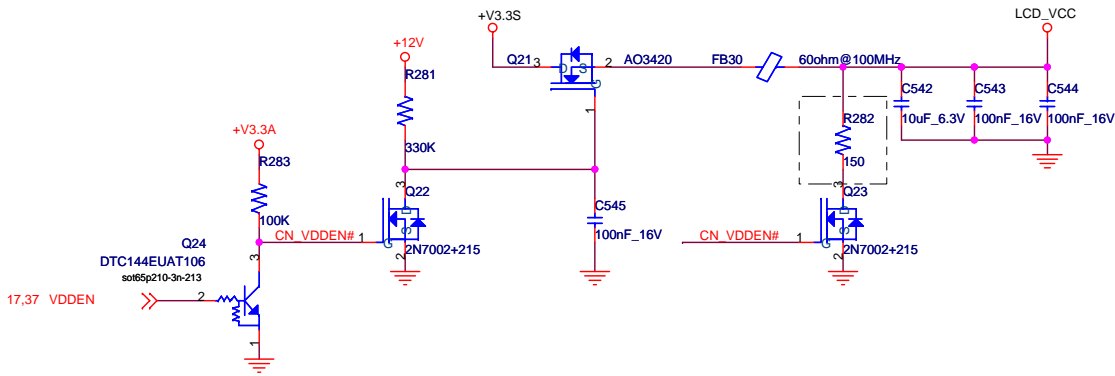




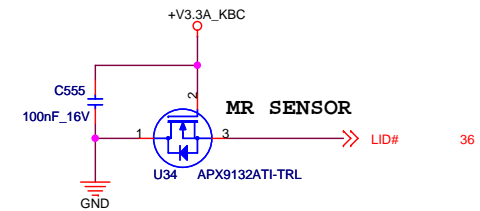
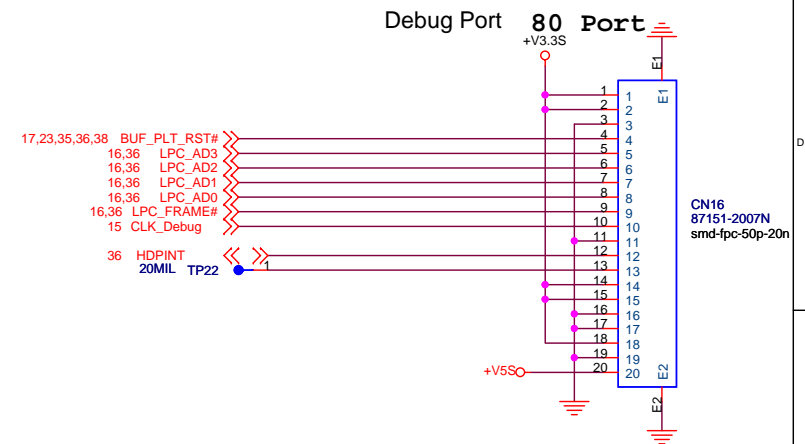
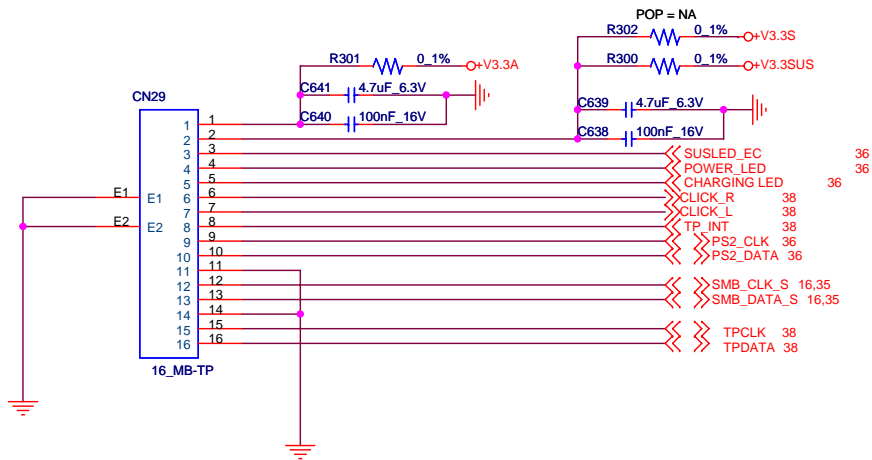
for FHD

7 TXCAM_DPA3N >> C473 100nF_16V TXCAM_CLK-
 7 TXCAP_DPA3P >> C474 100nF_16V TXCAM_CLK+
 7 TXOM_DPA2N >> C475 100nF_16V TXOM_IN0-
 7 TXOP_DPA2P >> C476 100nF_16V TXOM_IN0+
 7 TX1M_DPA1N >> C477 100nF_16V TXOM_IN1-
 7 TX1P_DPA1P >> C478 100nF_16V TXOM_IN1+
 7 TX2M_DPA0N >> C479 100nF_16V TXOM_IN2-
 7 TX2P_DPA0P >> C480 100nF_16V TXOM_IN2+

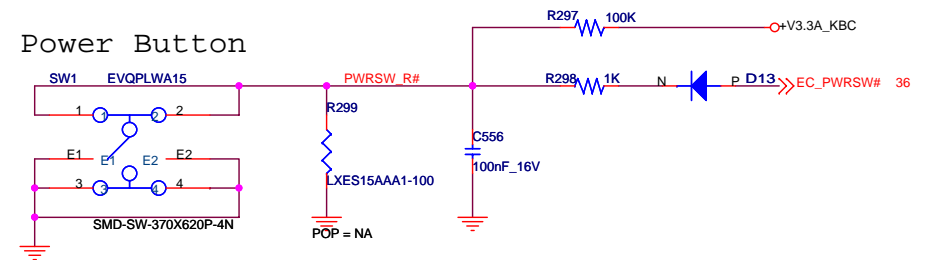
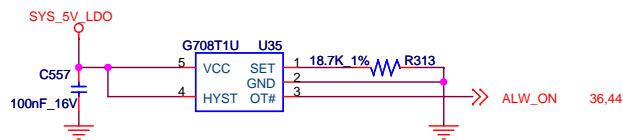




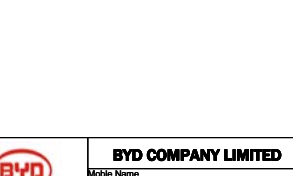
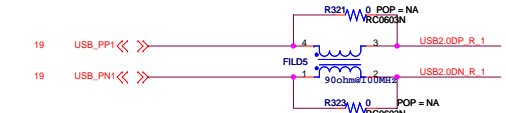
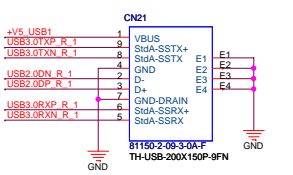
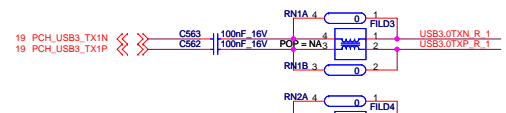
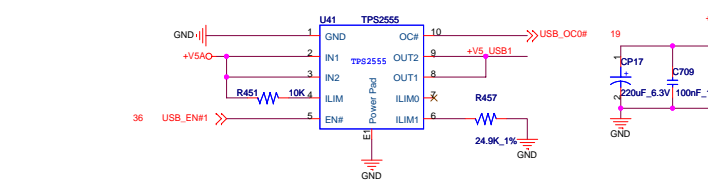
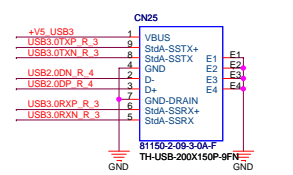
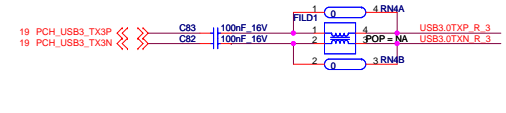
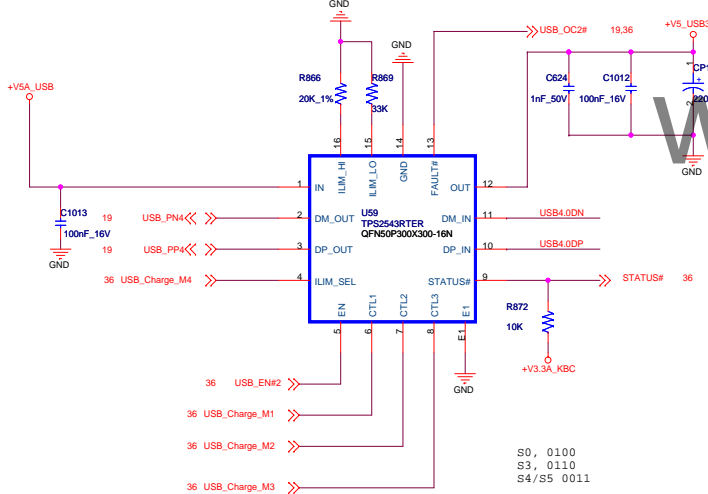
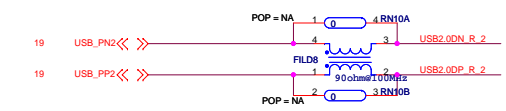
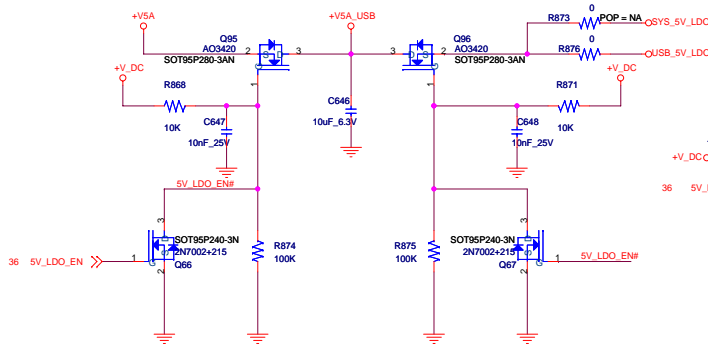
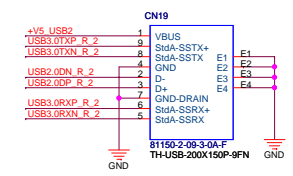
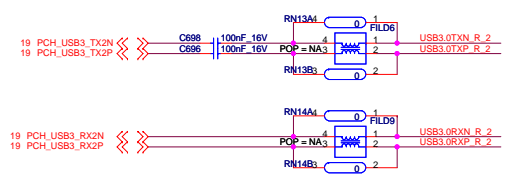
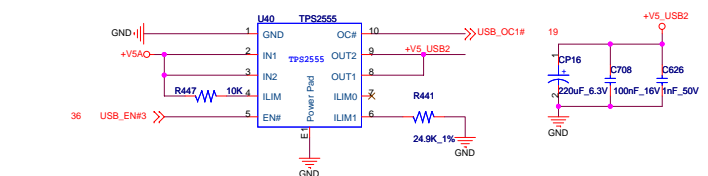
		BYD COMPANY LIMITED	
		Mobile Name: Betty	
Page Name: LVDS		Rev: V1.0	
Date: Sunday, May 05, 2013		Sheet: 40 of 51	



www.aitech1.ru

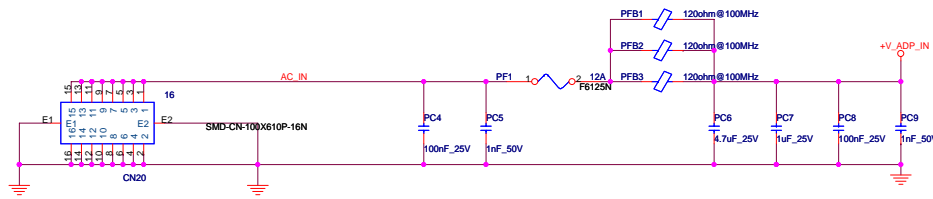


	BYD COMPANY LIMITED	
	Moble Name	Betty
Page Name	TP/LED/Power switch	Rev
Date: Sunday, May 05, 2013	Sheet 41 of 51	V1.0

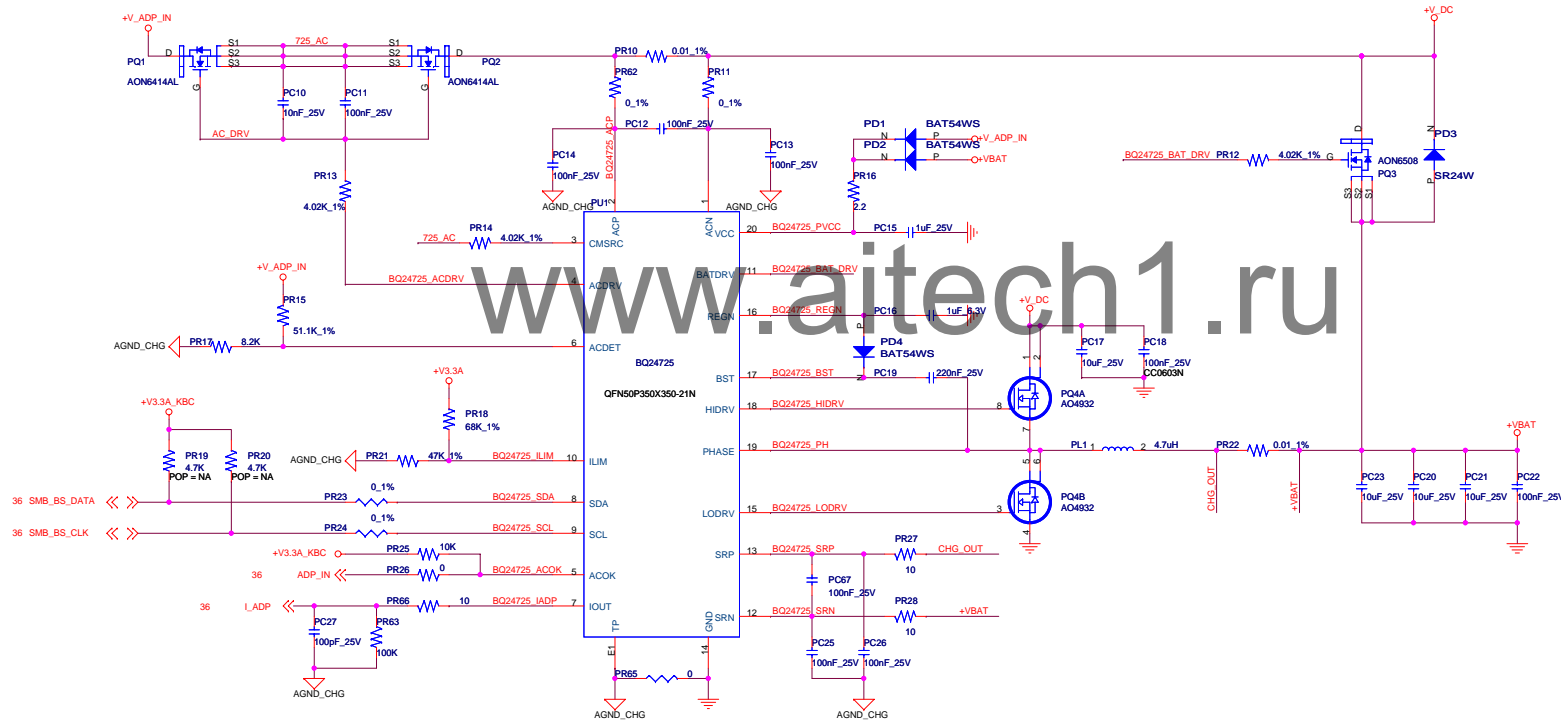
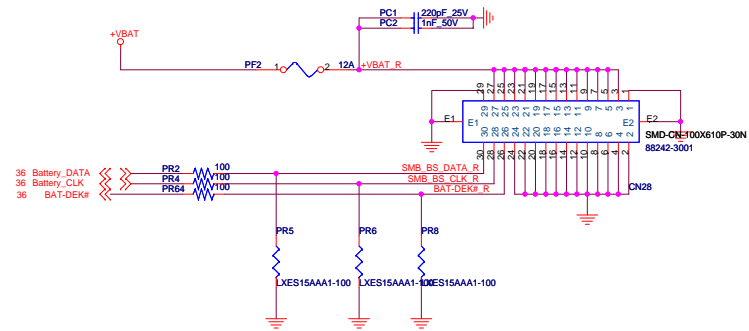


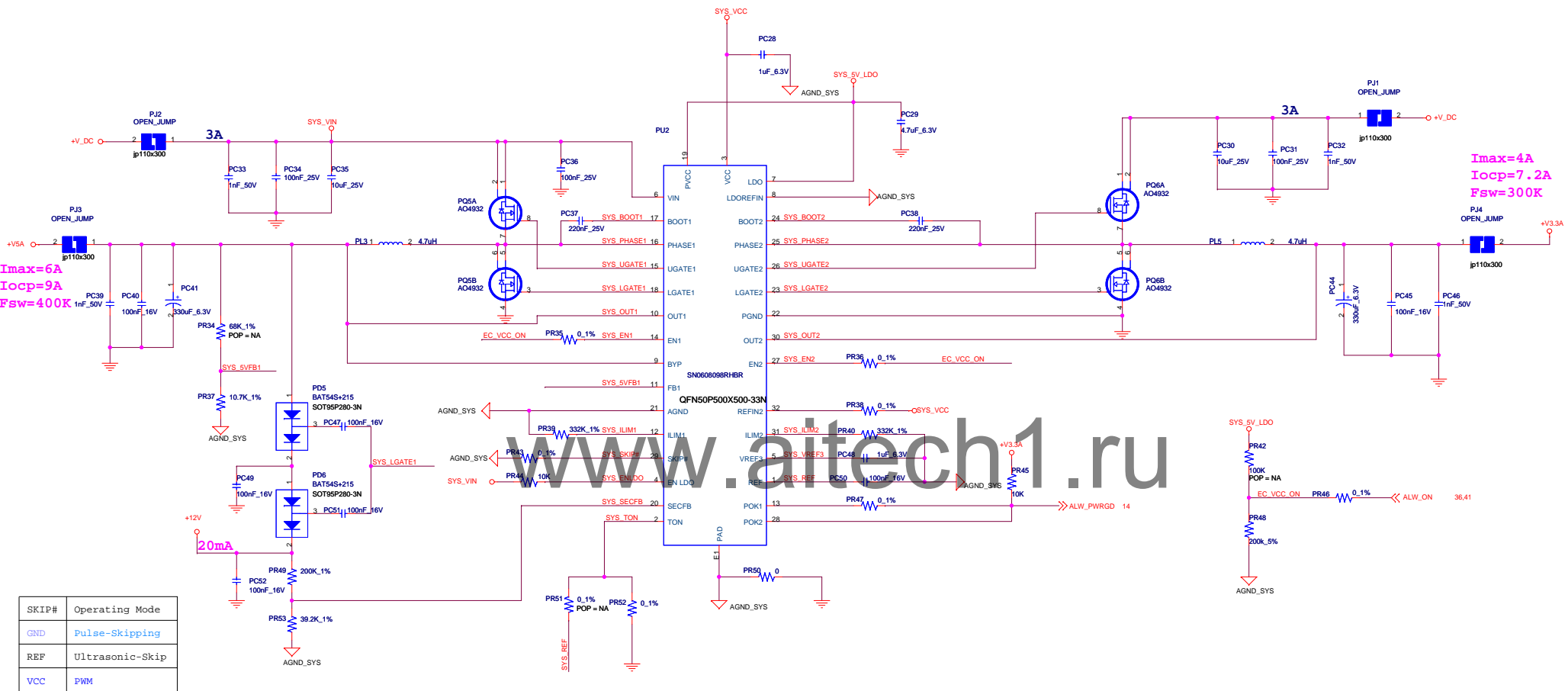
www.aitech1.ru

ADPTER_CON



BATTERY_CON





Imax=6A
Iocp=9A
Fsw=400K

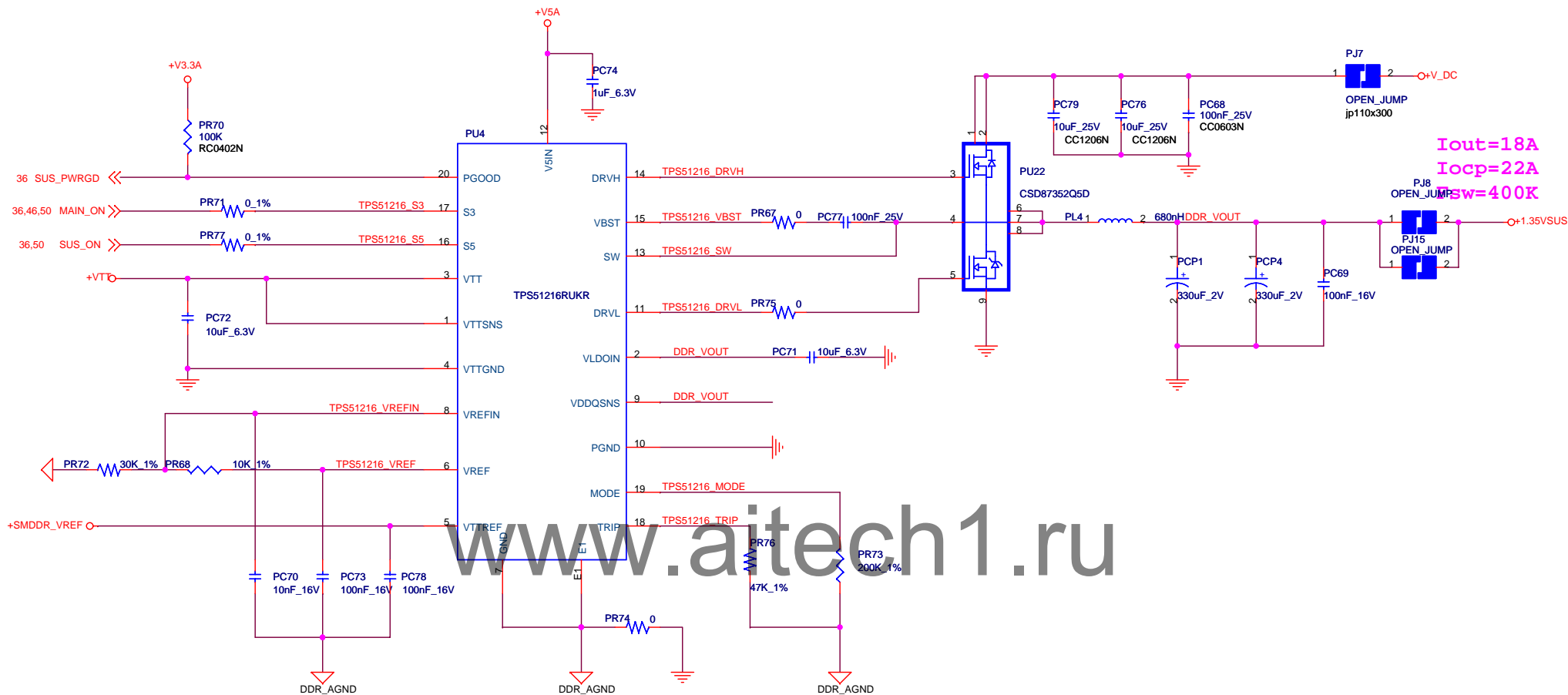
Imax=4A
Iocp=7.2A
Fsw=300K

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

Second Feedback :
 $V_{out_sec} = 12V$, $R2 = 39.2K$
 $R1 = R2 \times (V_{out_sec} / 2V - 1) = 200K$


Adjustable output of SMPS1:
 $V_{out1} = 5.1V$
 $R2 = 10K$, $R1 = R2 \times (V_{out1} / 0.7V - 1) = 62.9K$

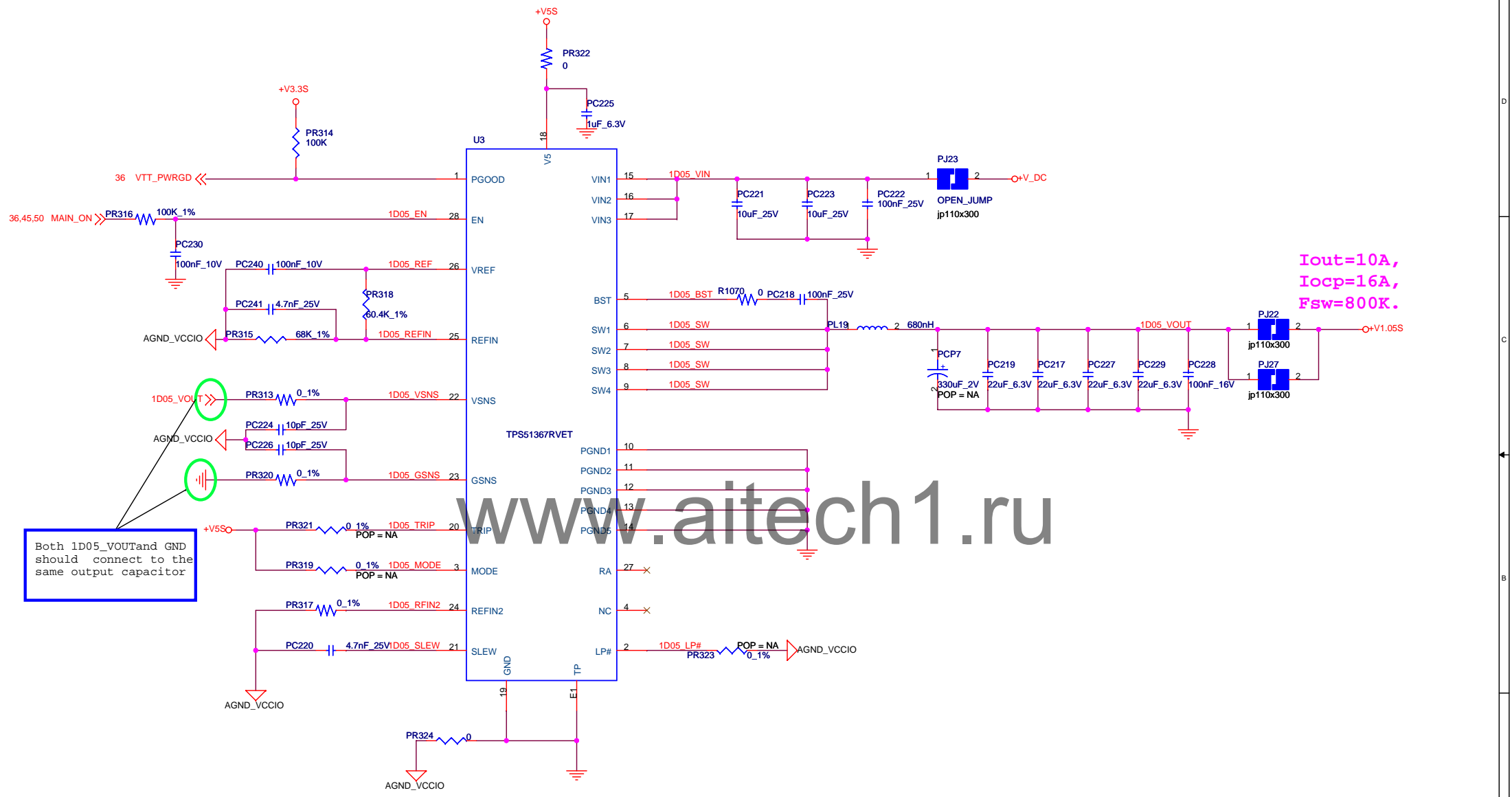
TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz



$I_{out}=18A$
 $I_{ocp}=22A$
 $R_{sw}=400K$

www.aitech1.ru

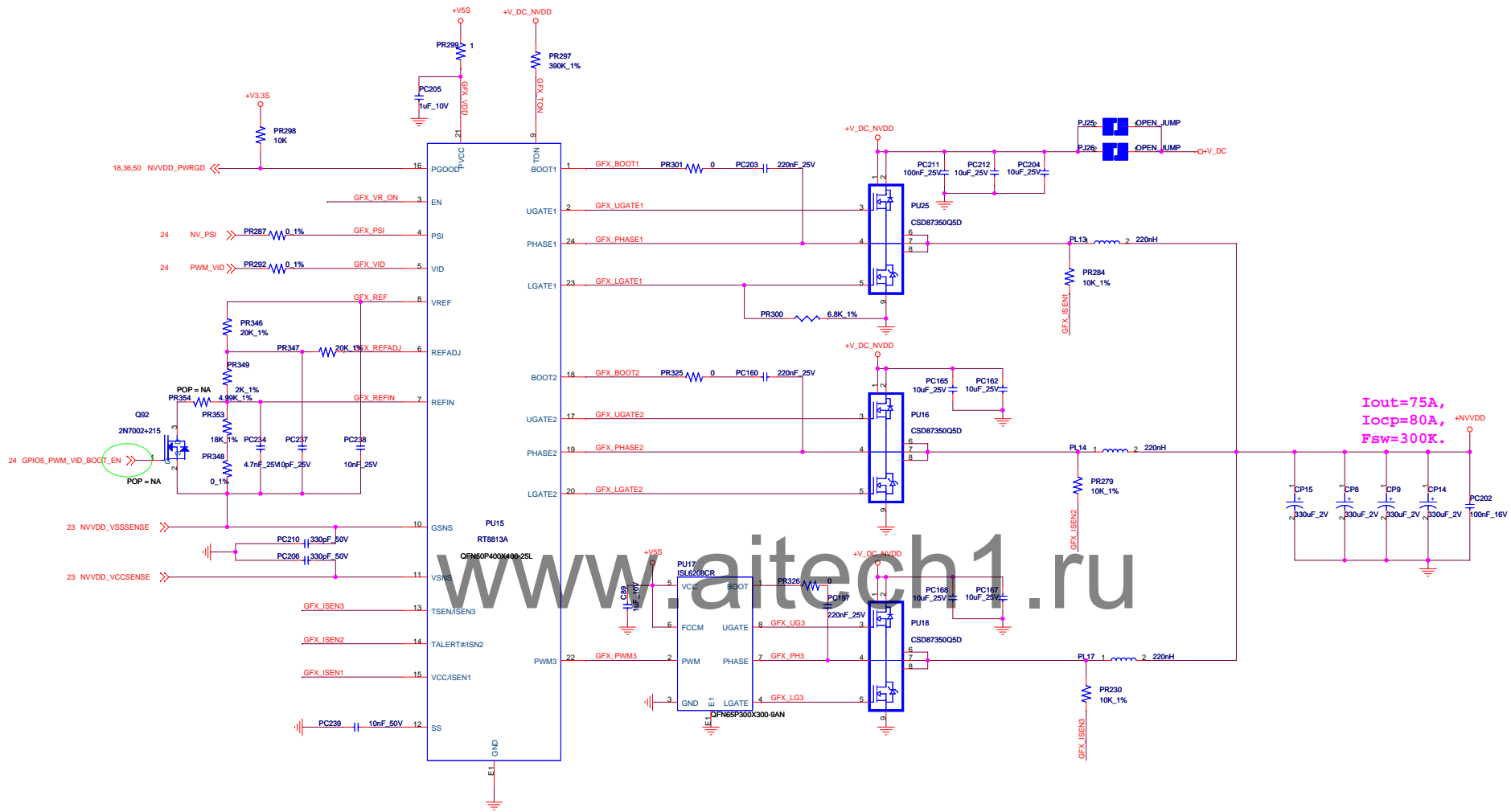
	BYD COMPANY LIMITED		
	Moble Name Betty		
Page Name	POWER DDR3L		Rev
Date: Sunday, May 05, 2013	Sheet 45	of 51	V1.0



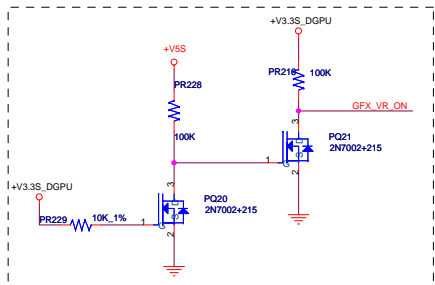
$I_{out}=10A,$
 $I_{ocp}=16A,$
 $F_{sw}=800K.$

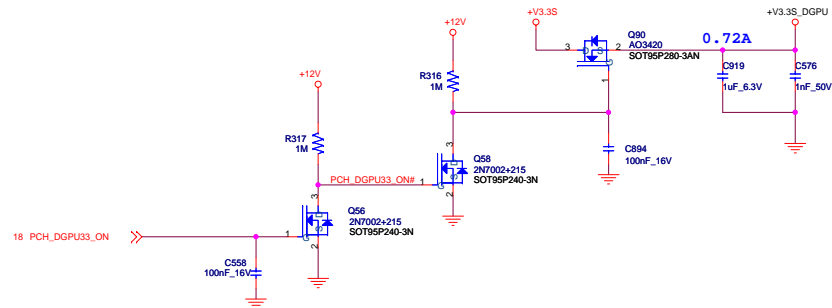
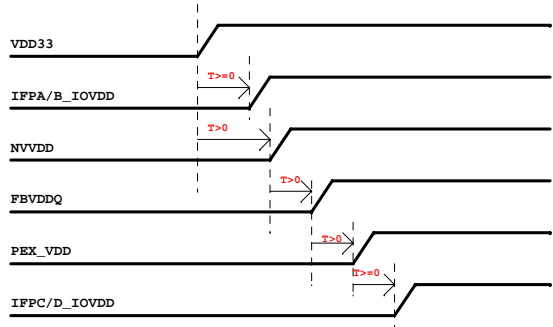
Both 1D05_VOUT and GND should connect to the same output capacitor

www.aitech1.ru

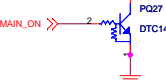
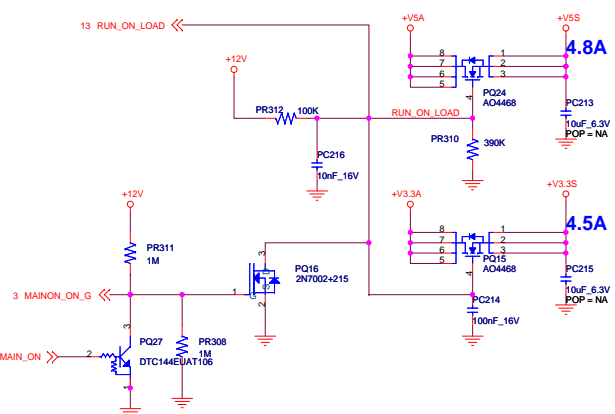
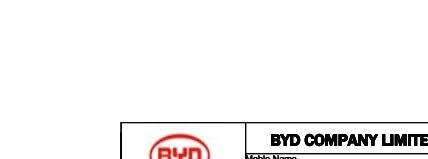
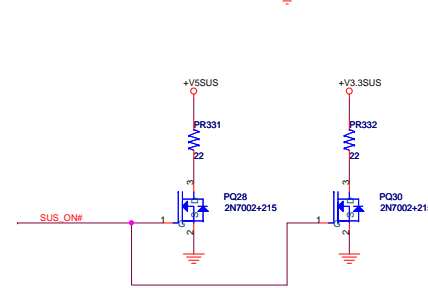
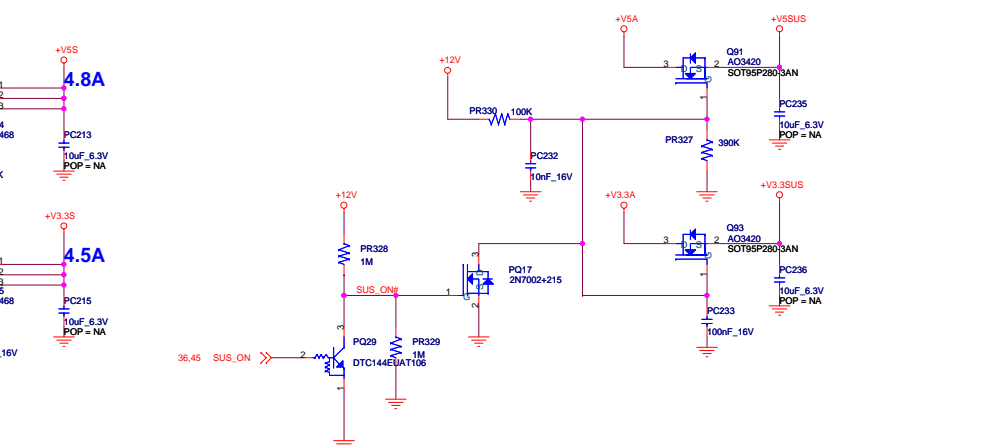
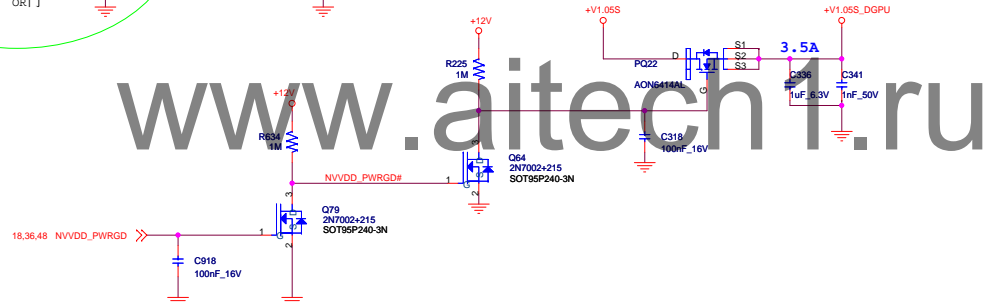
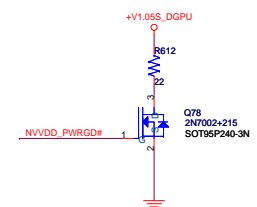
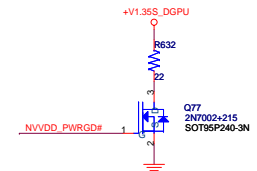
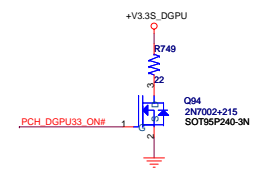
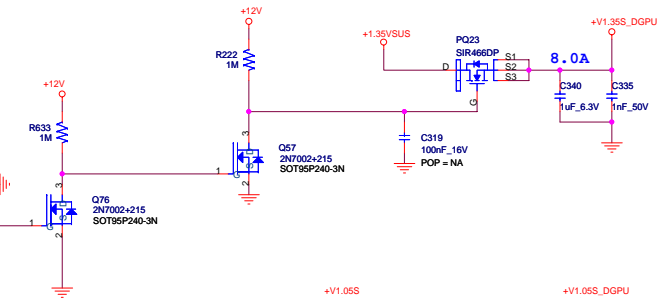
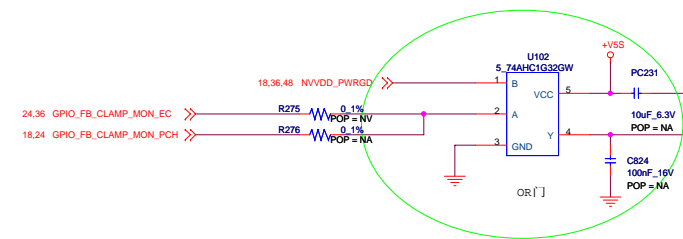
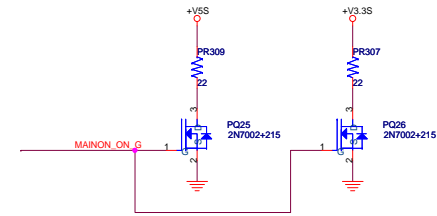


$I_{out}=75A$,
 $I_{ocp}=80A$,
 $F_{sw}=300K$.

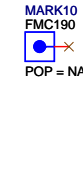
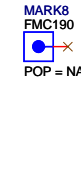
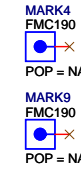
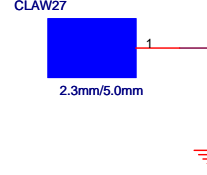
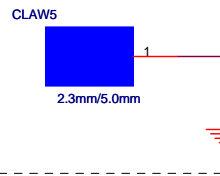
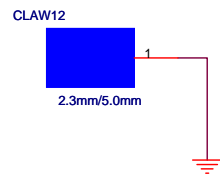
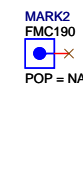
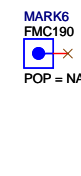
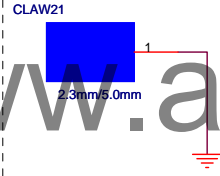
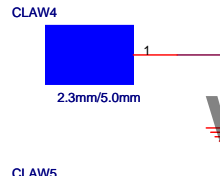
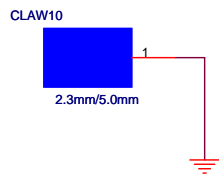
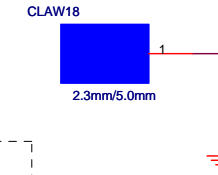
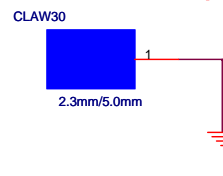
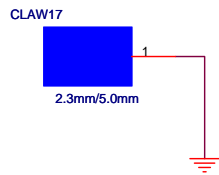
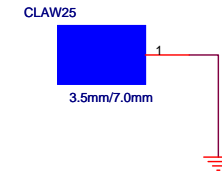
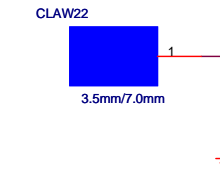
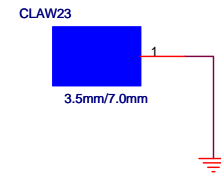
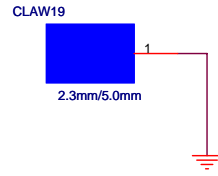
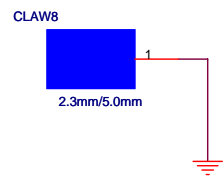
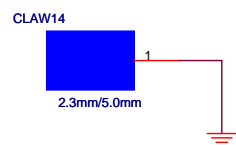
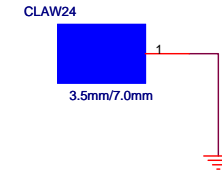
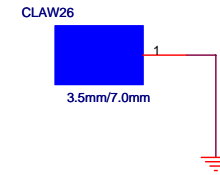
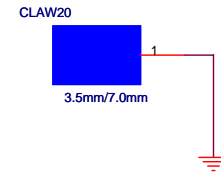
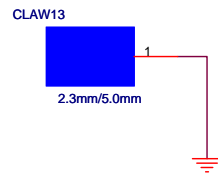
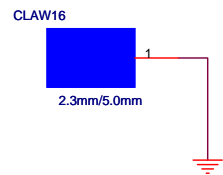
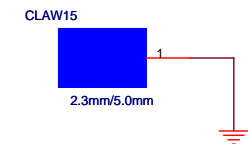




Power Discharge Circuit



www.aitech1.ru



	BYD COMPANY LIMITED	
	Mobile Name Betty	
Page Name	ME	Rev
Date: Sunday, May 05, 2013	Sheet 51 of 51	V1.0